KLE Technological University
Creating Value
Leveraging Knowledge

Linear Integrated Circuits

19EECC203

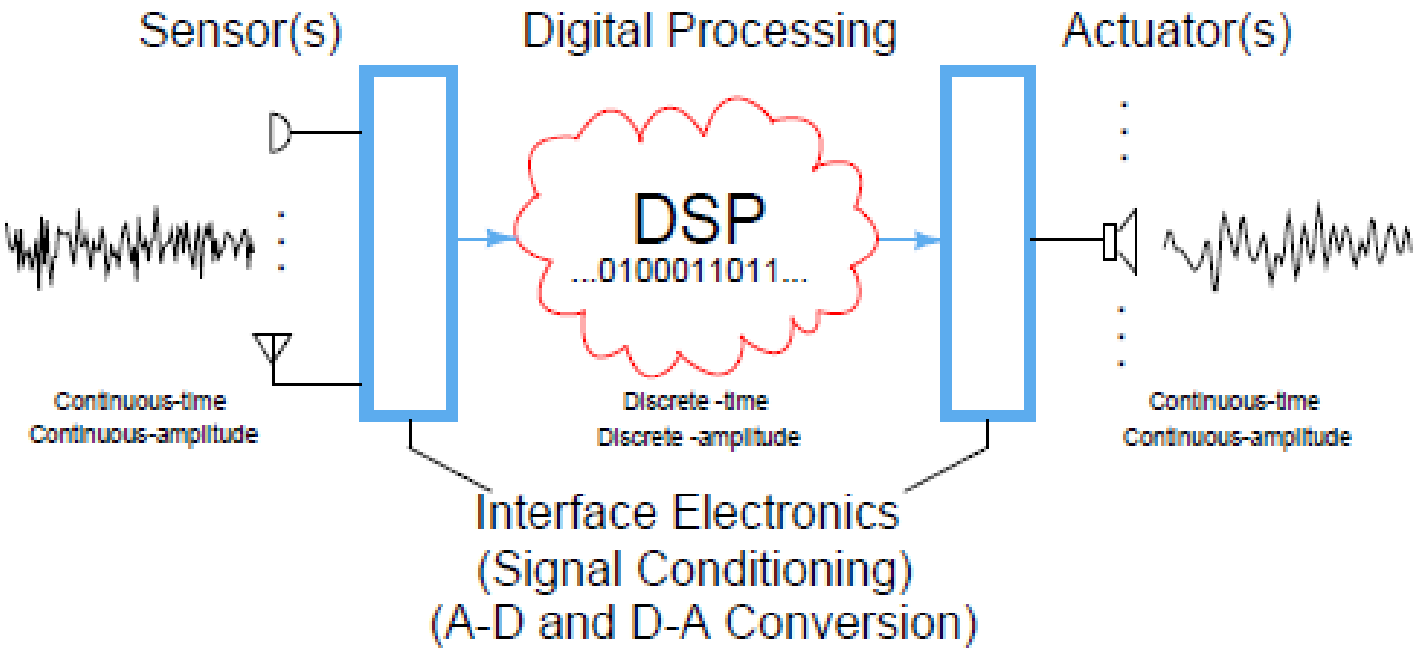
Unit: III

Chapter No: 06

Non-Linear Applications - Data Converters

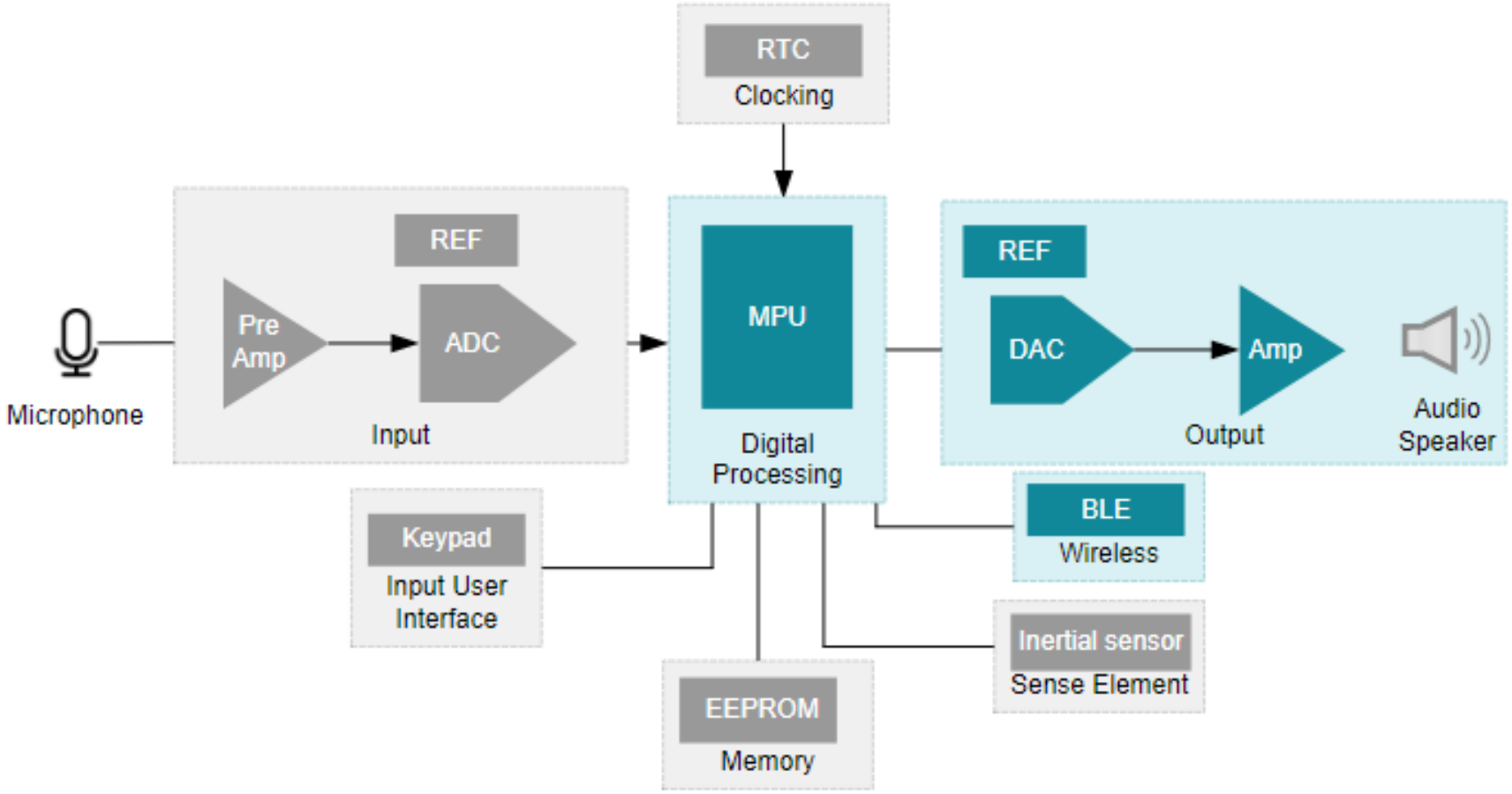
Resource Person: Dr Sujatha Sanjay Kotabagi

Data Converters



Data converter circuits (ADC and DAC) are essential blocks for interfacing the analog world and digital systems.

Data Converters for Audio Range Applications



Data Converters

- ***Applications such as wireless communications and digital audio and video have created the need for cost-effective data converters that will achieve higher speed and resolution.***
- ***The needs required by digital signal processors continually challenge analog designers to improve and develop new ADC and DAC architectures.***
- ***There are many different types of architectures, each with unique characteristics and different limitations.***

Types of Data converters

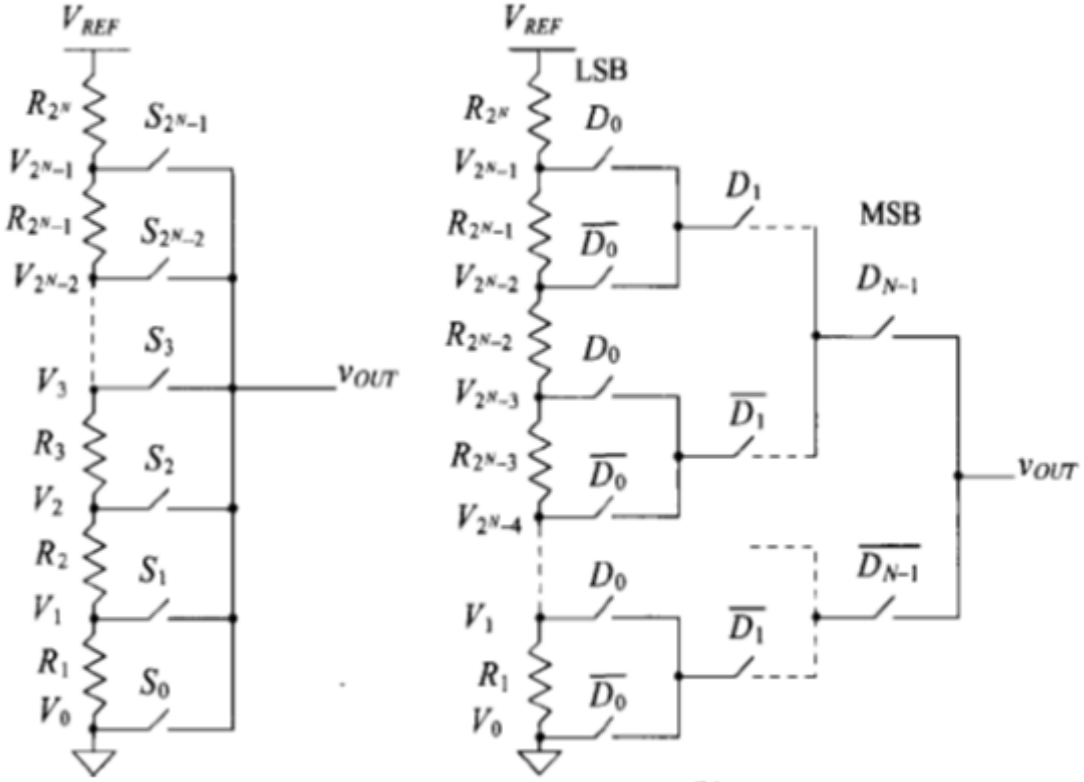
DACs

1. *Resistor String*
2. *R-2R*
3. *Current Steering*
4. *Cyclic*
5. *Pipeline*

ADCs

1. *Flash*
2. *Pipeline*
3. *Integrating - single slope*
   - dual slope
4. *SAR*

Resistor String DAC



1. *Resistor string of 2^N identical resistors and switches.*

2. *N:2^N decoder is required to provide the 2^N signals to control the switches.*

3. *The analog output is simply the voltage division of the resistors at the selected tap.*

4. *2^N - 1 switches are off and one switch is on. For larger resolutions, a large parasitic capacitance appears at the output node, resulting in slower conversion speeds.*

5. *Alternative for the resistor-string DAC is a binary switch array which ensures that the output is connected to at most N switches that are on and N switches that are off, thus increasing conversion speed*.

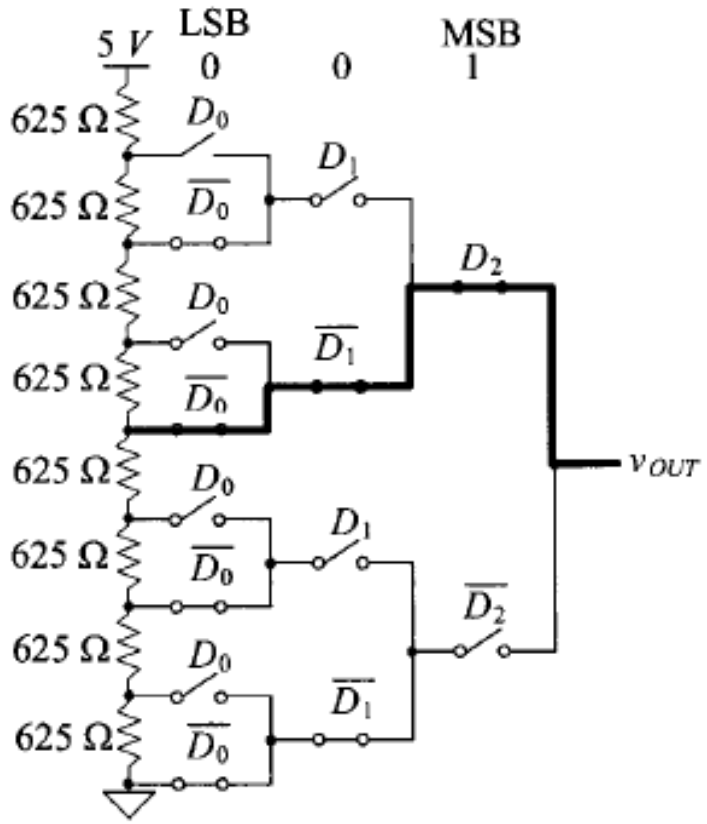
Data Converters

Ex. Design a 3 bit converter with V_{REF} = 5 V and maximum power dissipation of the converter of 5 mW

$$I_{MAX} = \frac{5 \times 10^{-3}\ \text{W}}{5\ \text{V}} = 1\ \text{mA}$$

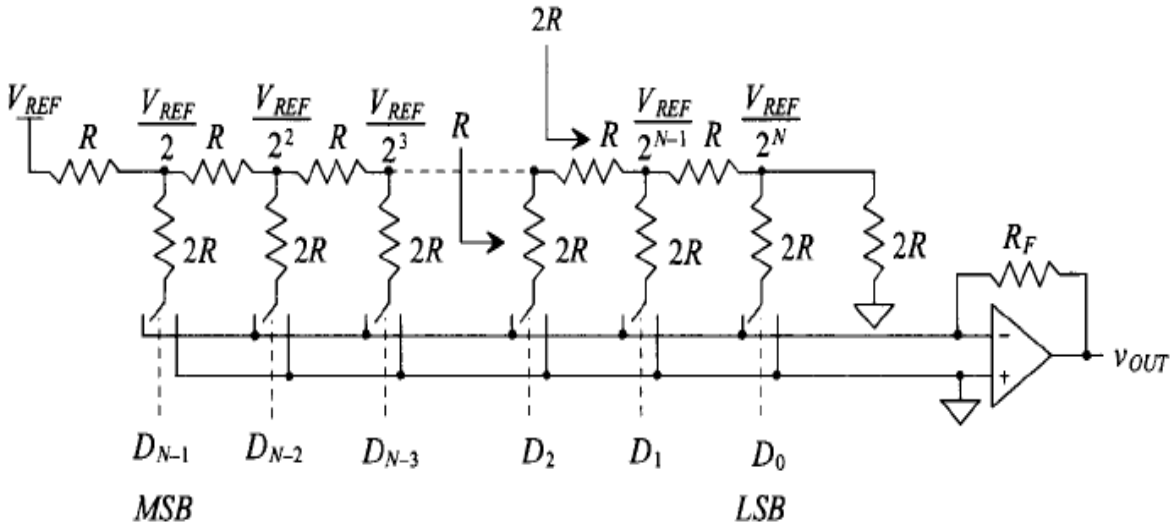
$$R = \frac{1}{8} \cdot \frac{5\ \text{V}}{1\ \text{mA}} = 625\ \Omega$$

$$D_2D_1D_0 = 100 \text{ or } 4_{10}.$$



$D_2D_1D_0$	v_{OUT}
000	0
001	0.625
010	1.25
011	1.875
100	2.5
101	3.125
110	3.75
111	4.375

R-2R Ladder Network



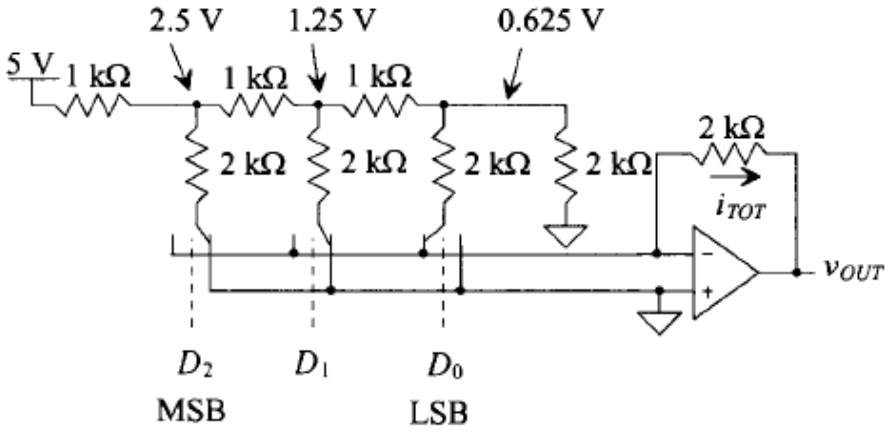
$$v_{OUT} = -i_{TOT} \cdot R_F$$

$$i_{TOT} = \sum_{k=0}^{N-1} D_k \cdot \frac{V_{REF}}{2^{N-k}} \cdot \frac{1}{2R}$$

where Dk is the k-th bit of the input word with a value that is either a 1 or a 0.

1. *It is a network of resistors alternating in value of R and 2R.*
2. *The resistance looking to the right of any node to ground is 2R.*
3. *The digital input determines whether each resistor is switched to ground (non-inverting input) or to the inverting input of the op- amp.*
4. *Each node voltage is related to V_{REF}, by a binary-weighted relationship caused by the voltage division of the ladder network.*
5. *The total current flowing from V_{REF} is constant, since the potential at the bottom of each switched resistor is always zero volts (either ground or virtual ground).*

Ex. Design a 3-bit DAC using an R-2R architecture with R = 1 kΩ, R_F = 2 kΩ, and V_{REF}= 5 V. Assume that the resistances of the switches are negligible. Determine the value of i_{TOT} for each digital input and the corresponding output voltage, v_{OUT}.



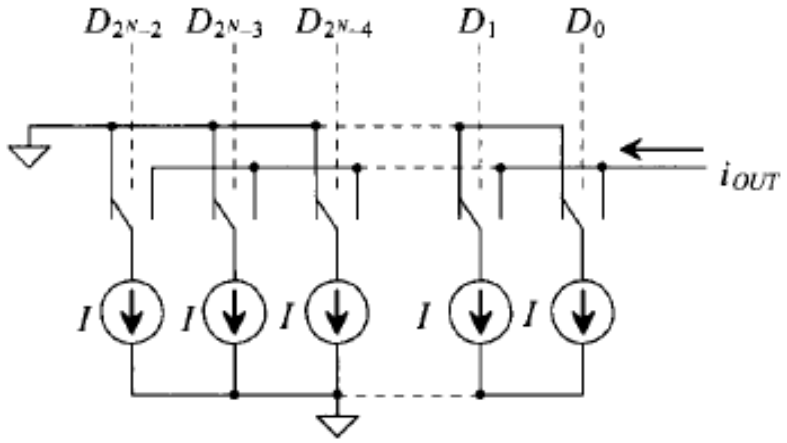
$D_2D_1D_0$	i_{TOT} (mA)	v_{OUT} (V)
000	0	0
001	0.3125	– 0.625
010	0.625	– 1.25
011	0.625 + 0.3125 = 0.9375	– 1.875
100	1.25	– 2.5
101	1.25 + 0.3125 = 1.5625	– 3.125
110	1.25 + 0.625 = 1.875	– 3.75
111	1.25 + 0.625 + 0.3125 = 2.1875	– 4.375

$D_2D_1D_0 = 001$ $\quad i_{TOT} = \dfrac{V_{REF}}{8} \cdot \dfrac{1}{2000} = 0.3126 \text{ mA}$

$$v_{OUT} = -(0.3126 \text{ mA})(2000\ \Omega) = -0.625 \text{ V}$$

Current Steering DAC

Another DAC method uses current throughout the conversion. Known as current steering, this type of DAC requires precision current sources that are summed in various fashions.



A generic current-steering DAC.

1. ***This configuration requires a set of current sources, each having a unit value of current, I.***

2. ***Since there are no current sources generating i_{OUT} when all the digital inputs are zero, the MSB, D_{2^N-1}, is offset by two index positions instead of one. For a 3-bit converter, seven current sources will be needed, labeled from D0 to D6.***

3. ***The binary signal controls whether or not the current sources are connected to either i_{OUT} or some other summing node (in this case ground).***

4. ***The output current, i_{OUT}, has the range of***

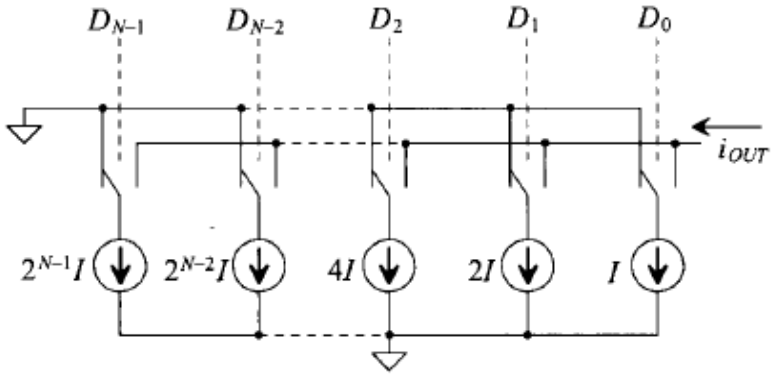
$$0 < Iout < (2^N-1)I$$

and can be any integer multiple of I in between.

5. ***There are 2^N - 1 current sources, the digital input will be in the form of a thermometer code.***

Data Converters

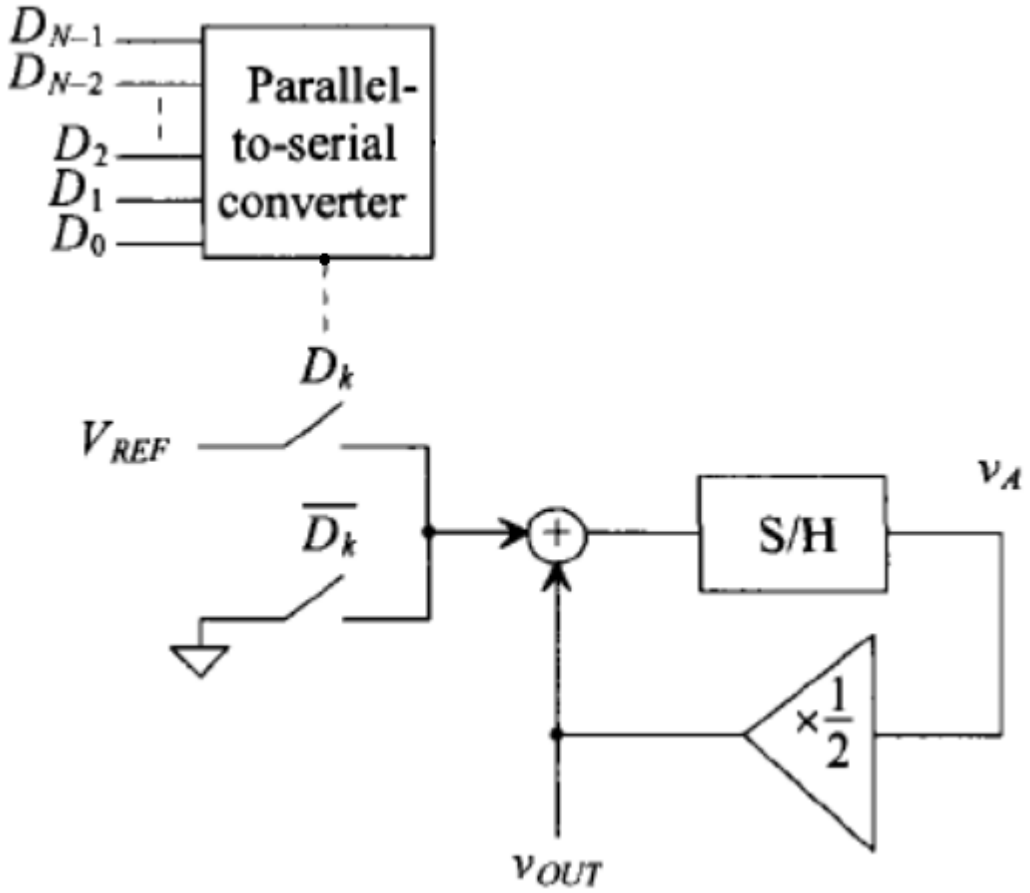
A current-steering DAC using binary-weighted current sources.



1. *This architecture uses binary-weighted current sources, thus requiring only N current sources of various sizes*

2. *The input code can be a simple binary number with no thermometer encoder needed.*

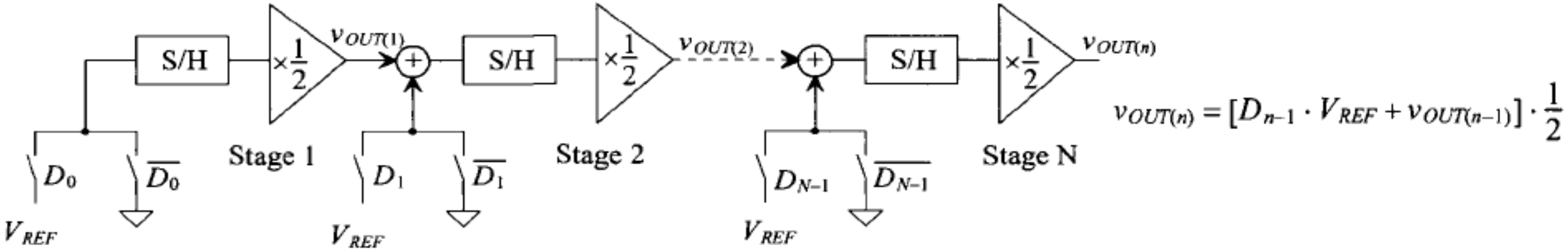
Cyclic DAC



1. *Inputs are read in serial fashion (PISO)*
2. *Summer adds V_{REF} or ground to the feedback signal depending on the input bits.*
3. *An amplifier with a gain of 0.5 feeds the output voltage back to the summer*
4. *The output at the end of each cycle depends on the value of the output during the cycle before.*
5. *The conversion is performed one bit at a time, resulting in N cycles for each conversion.*

$$v_{OUT}(n) = \left(D_{n-1} \cdot V_{REF} + \frac{1}{2} \cdot v_A(n-1)\right) \cdot \frac{1}{2} \quad \text{and} \quad [v_A(0) = 0\ \text{V}].$$

Pipeline DAC



$$v_{OUT(n)} = [D_{n-1} \cdot V_{REF} + v_{OUT(n-1)}] \cdot \frac{1}{2}$$

1. Extend the cyclic converter to N stages, where each stage performs one bit of the conversion------Pipeline DAC

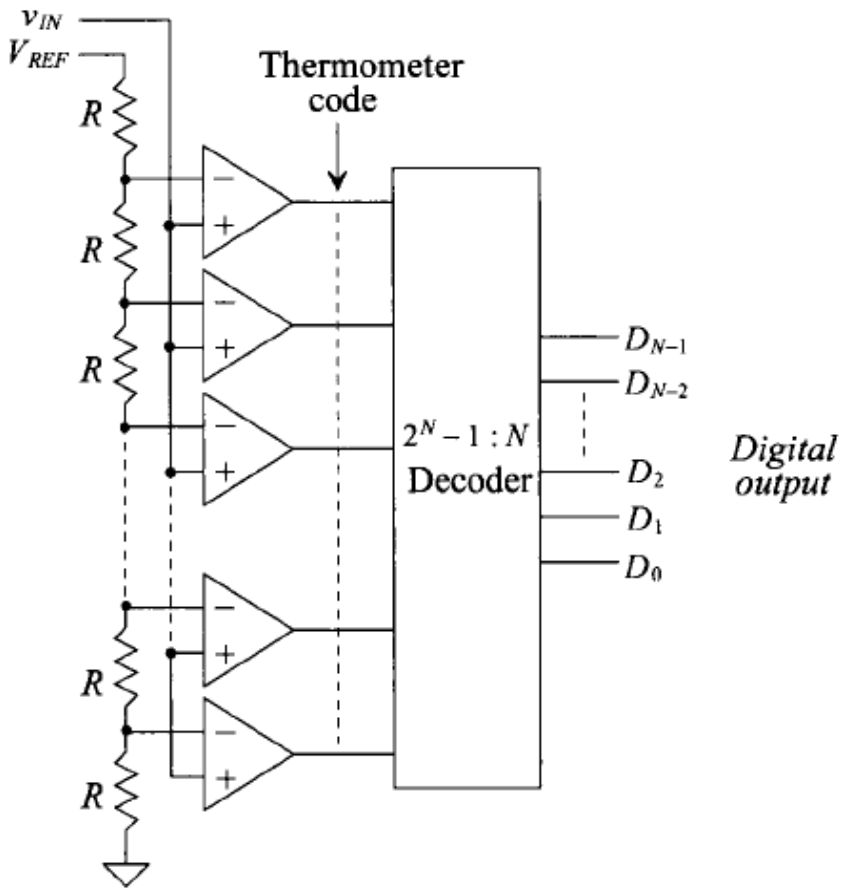
2. As each stage works on one conversion, the previous stage can begin processing another.
∴ Initial N clock cycle delay and there after one conversion per cycle

Operation of each stage:

- ***If the input bit is a 1, add V_{REF} to the output of the previous stage, divide by two, and pass the value to the next stage.***

- ***If the input bit is a 0, simply divide the output of the previous stage by two and pass along the resulting value.***

Flash ADC



1. One comparator per quantization level ($2^N - 1$) and 2^N resistors

2. The reference voltage is divided into 2^N values

3. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators

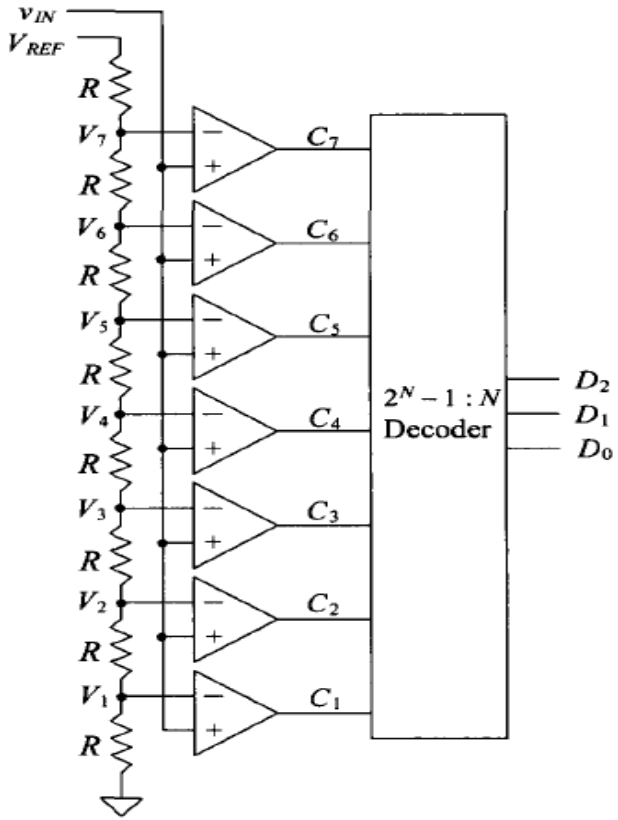
4. If v_{in} < value on the resistor string ; comp output = all zeros

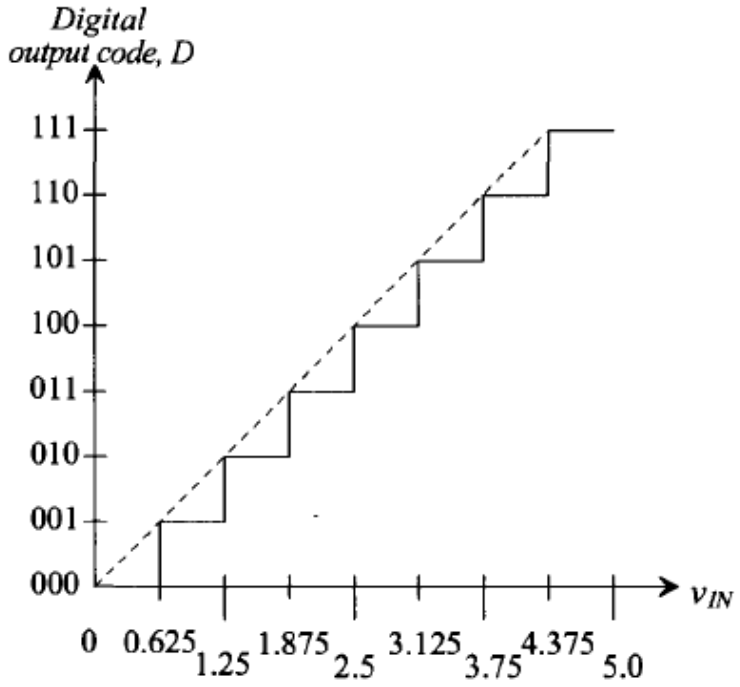
   v_{in} > value on the resistor string ; comp output = all ones

5. $2^N - 1$: N digital thermometer decoder circuit converts the compared data into an N-bit digital word

Data Converters

Ex. Design a 3-bit Flash converter, listing the values of the voltages at each resistor tap, and draw the transfer curve for v_{in}= 0 to 5 V. Assume v_{REF}= 5 V. Construct a table listing the values of the thermometer code and the output of the decoder for v_{in}=1.5, 3.0, and 4.5 V.



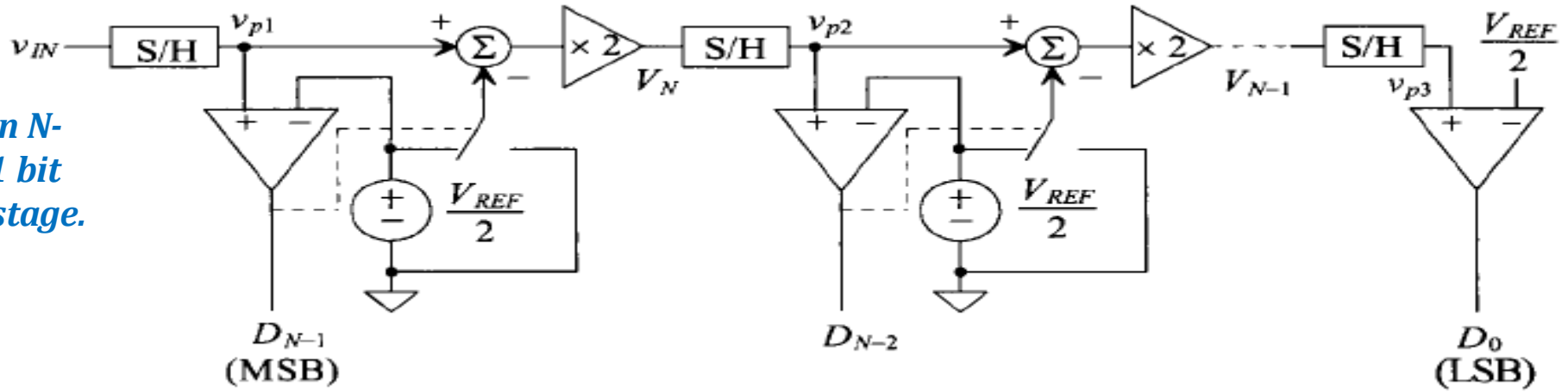


v_{IN}	$C_7C_6C_5C_4C_3C_2C_1$	$D_2D_1D_0$
$0 \le v_{IN} < 0.625$ V	0000000	000
0.625 V $\le v_{IN} < 1.25$ V	0000001	001
1.25 V $\le v_{IN} < 1.875$ V	0000011	010
1.875 V $\le v_{IN} < 2.5$ V	0000111	011
2.5 V $\le v_{IN} < 3.125$ V	0001111	100
3.125 V $\le v_{IN} < 3.75$ V	0011111	101
3.75 V $\le v_{IN} < 4.375$ V	0111111	110
$4.375 \le v_{IN}$	1111111	111

$V_1 = 0.625$ V, $V_2 = 1.25$ V, $V_3 = 1.875$ V, $V_4 = 2.5$ V, $V_5 = 3.125$, $V_6 = 3.75$ V, $V_7 = 4.375$ V.

Pipeline ADC

The pipeline ADC is an N-step converter, with 1 bit being converted per stage.



1. *After the input signal has been sampled, compare it to* $\frac{V_{REF}}{2}$. *The output of each comparator is the bit conversion for that stage.*

2. $If\ v_{in} > \frac{V_{REF}}{2}; comp\ output = 1; the\ difference\ \left(v_{in} - \frac{V_{REF}}{2}\right)\ is\ amplified$

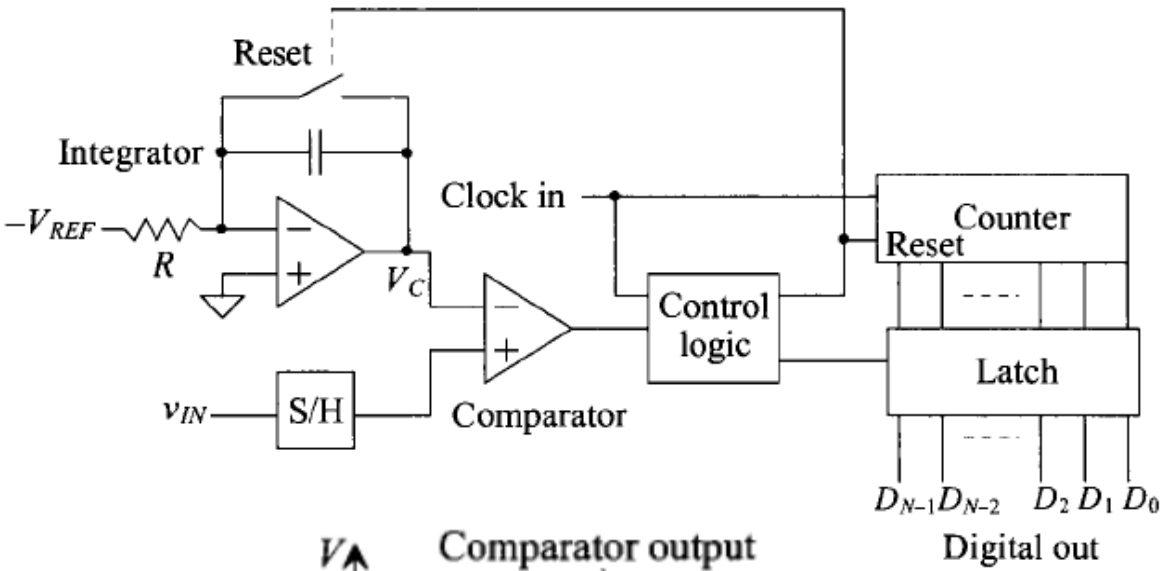
   $If\ v_{in} < \frac{V_{REF}}{2}; comp\ output = 0; only\ v_{in}\ is\ amplified.$

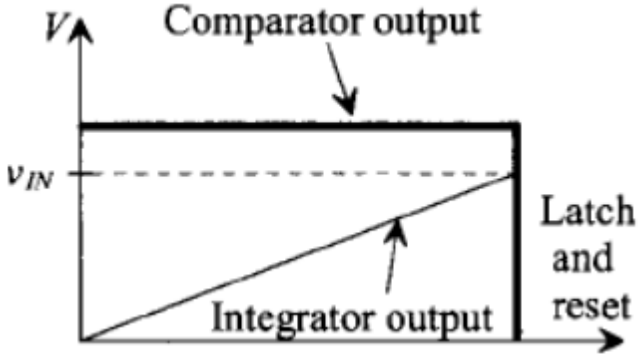
   The output of each stage in the converter is referred to as the residue

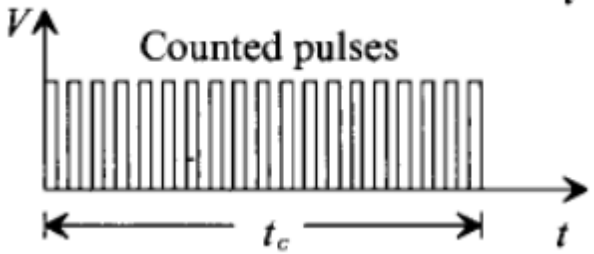
3. *Amplified signal is then passed to sample and hold of next stage*

Integrating ADC

- *Conversion is performed by integrating the input signal and correlating the integration time with a digital counter.*
- *Two types of Integrating ADCs: Single slope- and Dual-slope ADCs*
- *Used in high-resolution applications, slow-speed, cost-conscious applications.*







1. *The reference is a negative DC voltage, the output of the integrator should start at zero and linearly increase with a slope that depends on the gain of the integrator.*

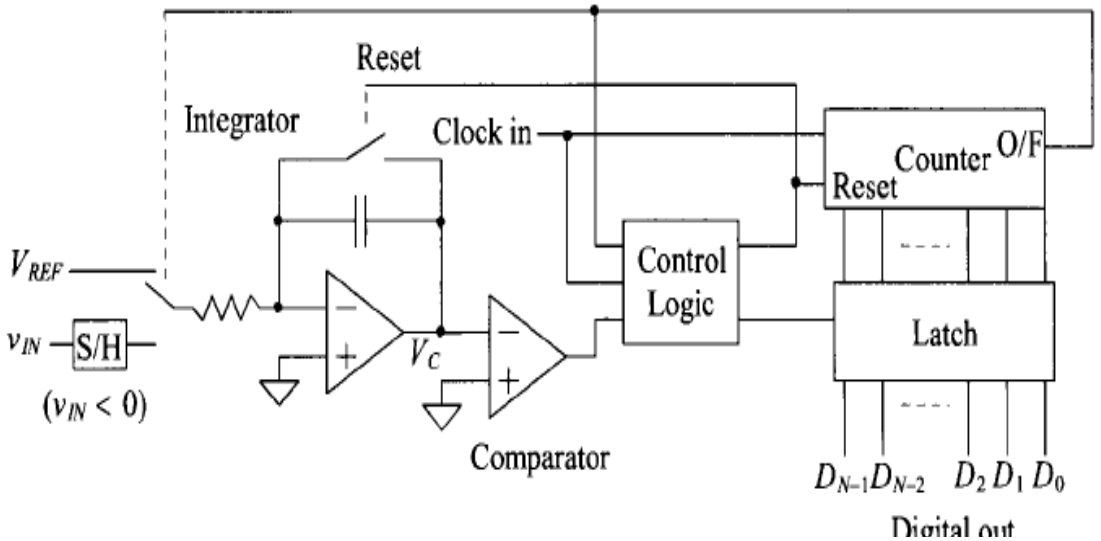
2. *At the time when the output of the integrator surpasses the value of the S/H output, the comparator switches states, thus triggering the control logic to latch the value of the counter.*

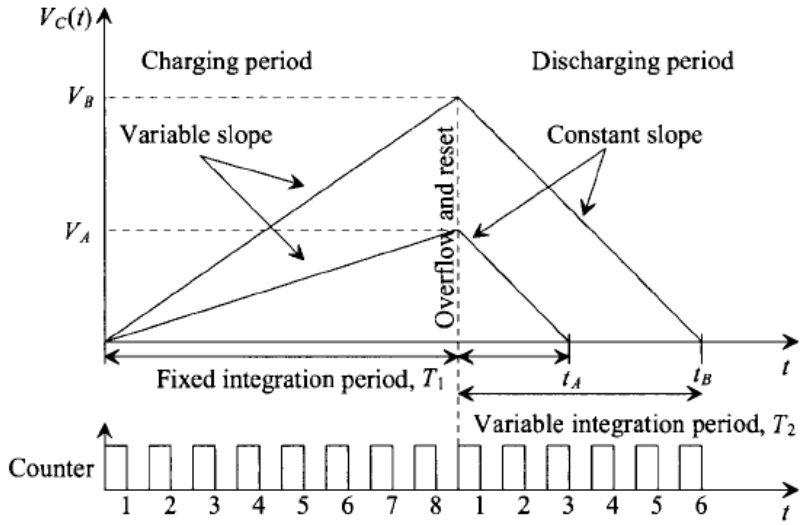
3. *The control logic also resets the system for the next sample.*

4. *If the input voltage is at its full-scale value, the counter must increment to its maximum value of 2^N clock cycles. Thus, the clock frequency must be many times faster than the bandwidth of the input signal.*

$$t_c = \frac{v_{IN}}{V_{REF}} \cdot 2^N \cdot T_{CLK} \qquad f_{sample} = \frac{V_{REF}}{V_{IN} \cdot 2^N} \cdot f_{CLK}$$

Integrating ADC -Dual slope





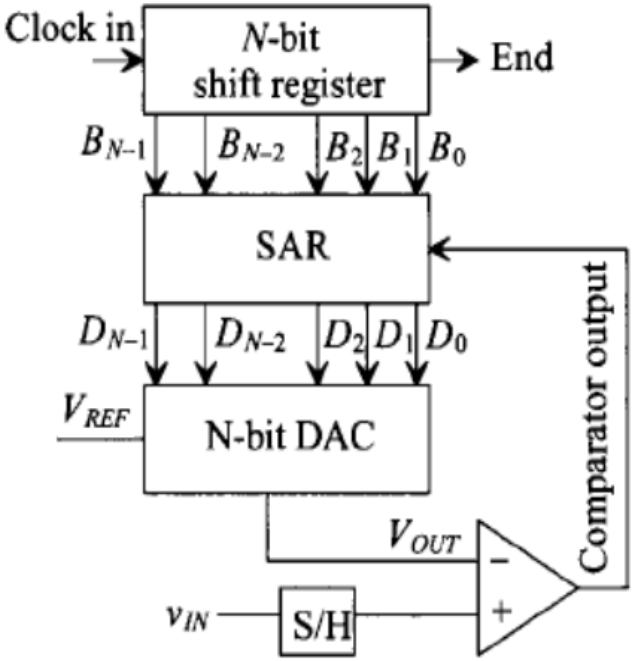
1. ***Two integrations are performed, one on the input signal and one on V_{REF}.***

2. ***The input voltage is assumed to be negative, and the output is a positive slope during the first integration (fixed length) dictated by counter.***

3. ***After the counter overflows and is reset, the reference voltage is connected to the input of the integrator, whose output discharges to zero at a constant slope.***

4. ***A counter again measures the amount of time for the integrator to discharge, thus generating the digital output.***

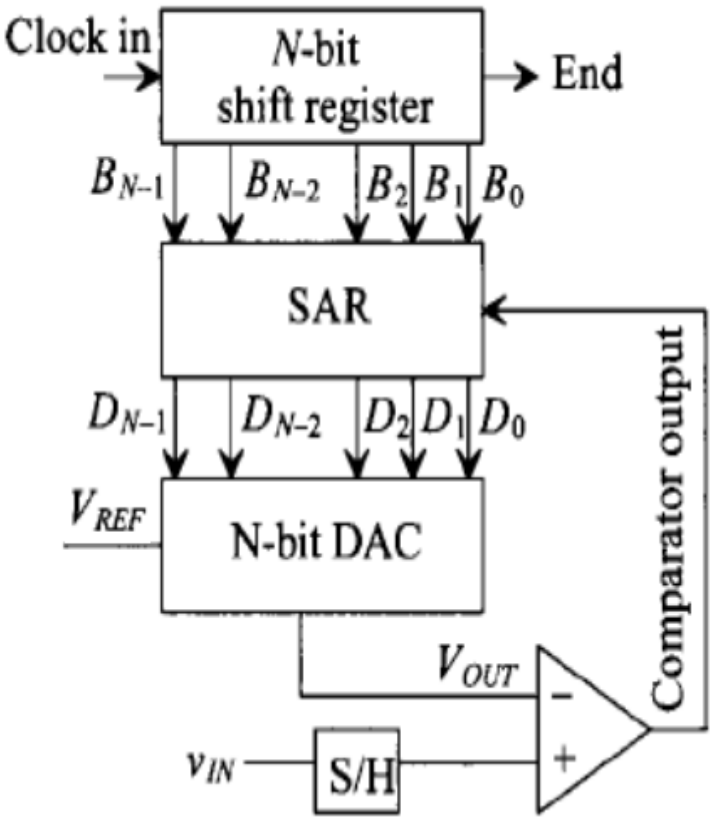
Successive Approximation ADC



- *The successive approximation converter performs basically a binary search through all possible quantization levels before converging on the final digital answer.*
- *An N-bit register controls the timing of the conversion where N is the resolution of the ADC.*
- *v_{IN} is sampled and compared to the output of the DAC.*
- *The comparator output controls the direction of the binary search, and the output of the successive approximation register (SAR) is the actual digital conversion.*

Successive Approximation ADC

Algorithm



1. A 1 is applied to the input of the shift register. For each bit converted, the 1 is shifted to the right 1-bit position. B_{N-1}= 1 and B_{N-2} through B_0= 0.

2. The MSB of the SAR, D_{N-1}, is initially set to 1, while the remaining bits, D_{N-2} through D_0, are set to 0.

3. Since the SAR output controls the DAC and the SAR output is 100...0, the DAC output will be set to $\frac{V_{REF}}{2}$.

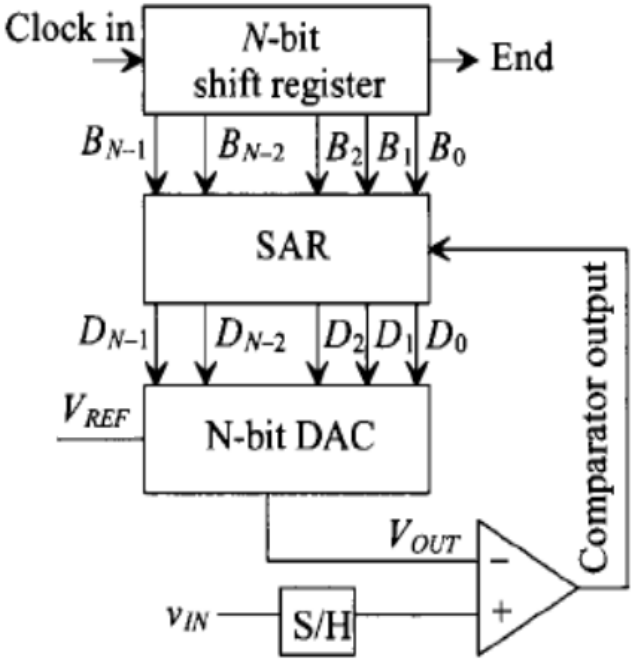
4. If $\frac{V_{REF}}{2} > v_{IN}$; comparator output = 0 and the comparator resets D_{N-1} to 0.
   If $\frac{V_{REF}}{2} < v_{IN}$; comparator output = 1 and the D_{N-1} remains a 1.
   D_{N-1} is the actual MSB of the final digital output code.

5. The 1 applied to the shift register is then shifted by one position so that B_{N-2} while the remaining bits are all 0.

6. D_{N-2} is set to a 1, D_{N-3} through D_0 remain 0, while D_{N-1} remains the value from the MSB conversion.
   The output of the DAC = $\frac{V_{REF}}{4}$ (if D_{N-1}= 0) or $\frac{3V_{REF}}{4}$ if (D_{N-1}=1)

Data Converters

Perform the operation of a 3-bit SAR ADC with V_{REF}= 8. Show the binary search algorithm of the converter for $v_{IN} = 5.5V$ and 2.5 V.



Step	v_{IN}	$B_2B_1B_0$	$D_2D_1D_0$	V_{OUT}	Comp Out	$D_2D_1D_0$
T1	5.5	100	100	1/2 V_{REF} = 4 V	0	100
T2	5.5	010	110	(1/2+1/4)V_{REF} = 6 V	1	100
T3	5.5	001	101	(1/2+1/8)V_{REF} = 5 V	0	101

Step	v_{IN}	$B_2B_1B_0$	$D'_2D'_1D'_0$	V_{OUT}	Comp Out	$D_2D_1D_0$
T1	2.5	100	100	1/2 V_{REF} = 4 V	1	000
T2	2.5	010	010	1/4 V_{REF} = 2 V	0	010
T3	2.5	001	011	(1/4+1/8)V_{REF} = 3 V	1	010

Reference

CMOS Circuit Design, Layout, and Simulation
R. Jacob Baker

Thank you

KLE TECH.

KLE Technological University

Creating Value

Leveraging Knowledge

Linear Integrated Circuits
19EECC203

Unit: III
Chapter No: 06
Non-Linear Applications

Faculty Incharge: Dr Sujata Sanjay Kotabagi

Problems on Non-Linear Applications of Op-Amp

KLE Technological University
Creating Value
Leveraging Knowledge

Course Outcome (CO): Design and analyze the non-linear applications of Op-Amp for the given specifications.

PO1.3.1 - Apply fundamentals of Electrical engineering principles and laws

PO1.4.1 - Apply principles of electronic device

PO1.4.2 - Ability to understand electronic circuits

PO2.1.2 - Identify engineering systems, variables, and parameters to solve the problems

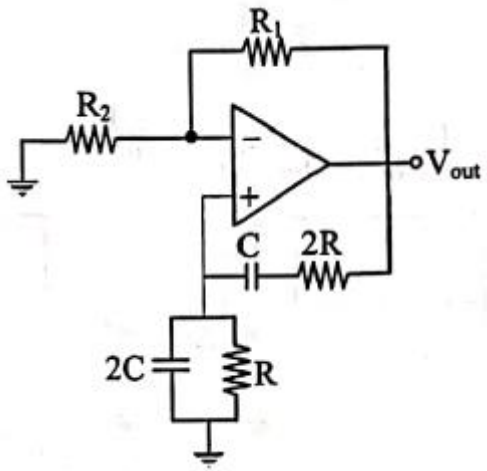
PO2.1.4 - Identify the mathematical, engineering and other relevant knowledge that applies to a given problem

Non-Linear Mode Applications

- **Output is saturated:** $v_o = \pm V_{o,sat}$
- **Differential input is :** $v_d \geq \frac{\pm V_{o,sat}}{A}$
- **Dominant positive feedback:** $\beta_- < \beta_+$

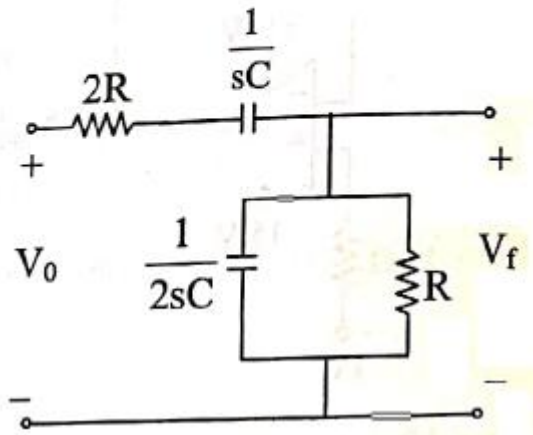
Problems on Non-Linear Applications of Op-Amp

P01: Determine the oscillation frequency and the condition to sustain oscillations for the circuit shown. Assume the Op-Amp to be ideal.



Gain, $|A| = \frac{R_1}{R_2} + 1$

Feedback network is, $\therefore \beta = \frac{V_f}{V_0}$



$$\therefore V_f = V_0 \frac{\left(R \,||\, \frac{1}{2sC}\right)}{\left(R \,||\, \frac{1}{2sC}\right) + \left(2R + \frac{1}{sC}\right)}$$

$$F = \frac{V_f}{V_0} = \frac{sCR}{4s^2C^2R^2 + 5sCR + 1}$$

For oscillations to occur

$[A\beta] = 1$

$[A] = \frac{1}{\beta}$

$$\therefore \text{So, } \left(1 + \frac{R_1}{R_2}\right) = \frac{4sC^2R^2 + 5sCR + 1}{sCR}$$

Put, $s = j\omega$, to get frequency of oscillations.

$$\therefore j\omega CR(R_1 + R_2) = R_2 + j\omega 5CRR_2 - 4\,\omega^2C^2R^2R_2$$

Let us compare imaginary parts

$$\therefore \omega\, CR(R_1 + R_2) = \omega 5CRR_2$$

$$\omega\, CRR_1 = \omega 5CR4R_2$$

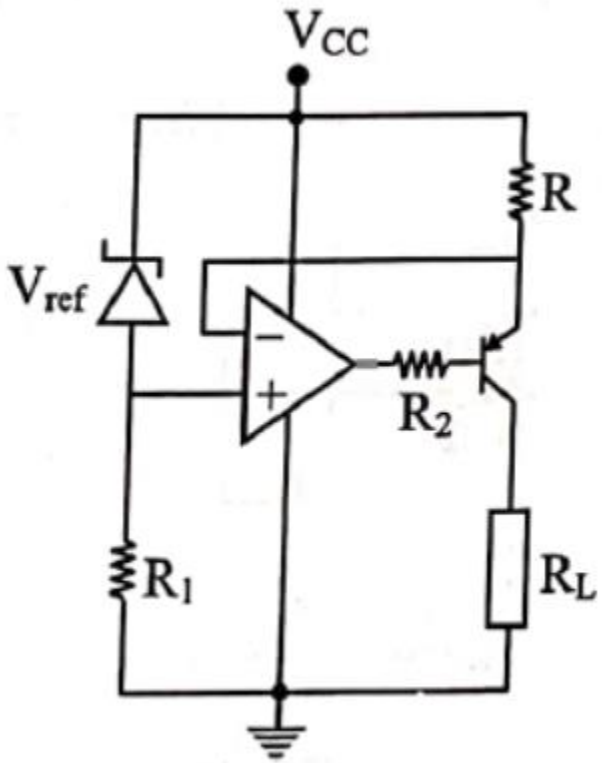
$R_1 = 4R_2$ and

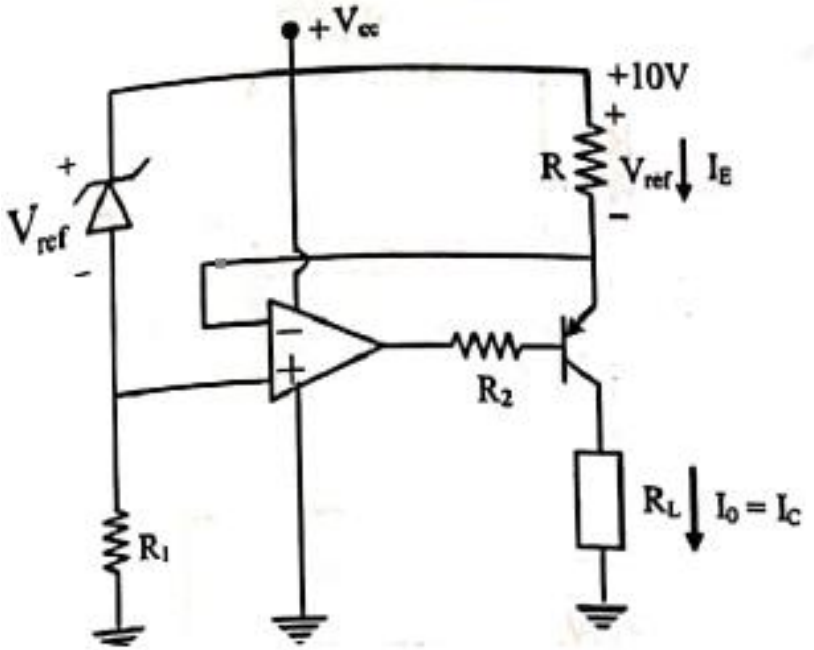
$$0 = R_2 - 4\omega^2C^2R^2R_2$$

$$\omega = \frac{1}{2CR}$$

Problems on Non-Linear Applications of Op-Amp

P02: Calculate the load current through R_L



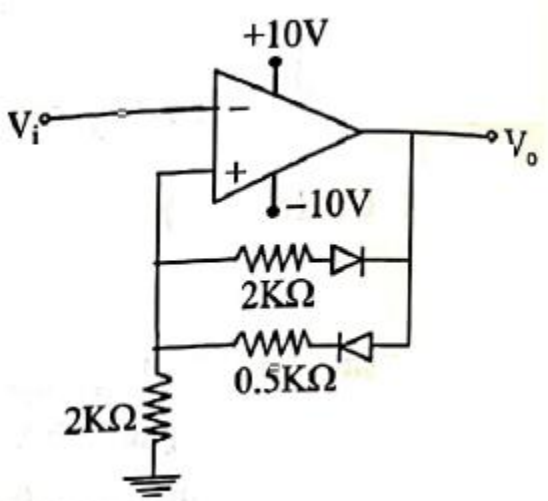


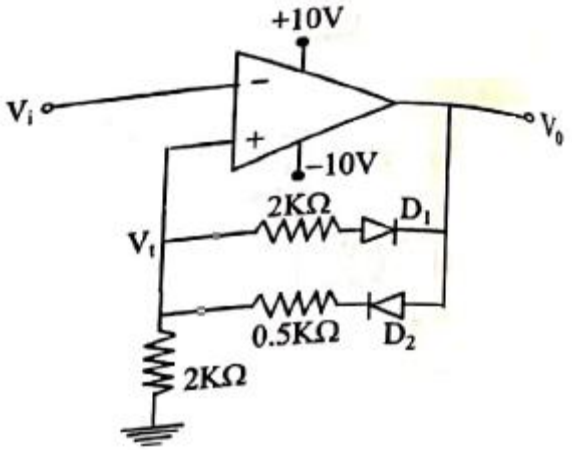
$V_p = V_N$ [Virtual short]

$$I_0 = I_C = \left(\frac{\beta}{\beta+1}\right) I_E = \left(\frac{\beta}{\beta+1}\right) \frac{V_{ref}}{R}$$

Problems on Non-Linear Applications of Op-Amp

P03: Plot the transfer characteristics of the circuit shown. Assume ideal diodes





$V_t = L_{tp}$ when $V_0 = -10V$

$$L_{tp} = \frac{-10 \times 2K}{(2+2)K}$$

$$= \frac{-20}{4}$$

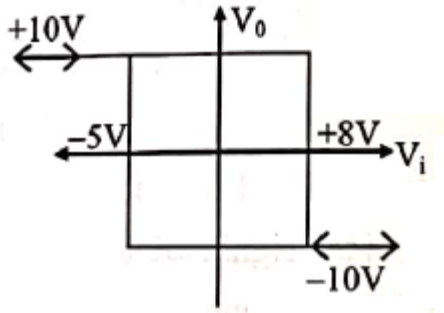
$$L_{tp} = -5V$$

$V_t = U_{tp}$ when $V_0 = +10V$

When diode D_2 is Forward bias

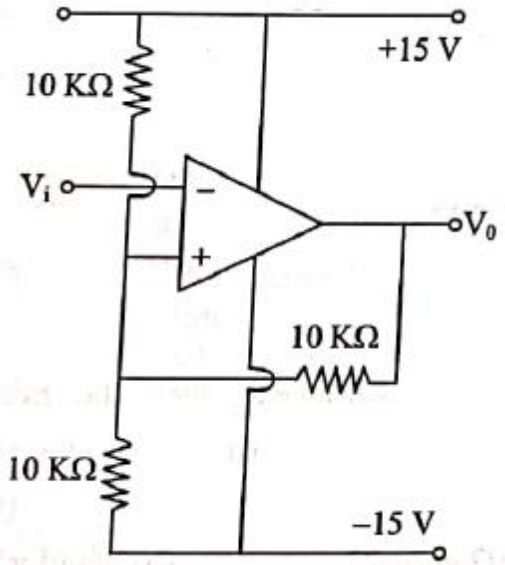
$$U_{tp} = \frac{10 \times 2K}{0.5k + 2K} = \frac{20}{2.5}$$

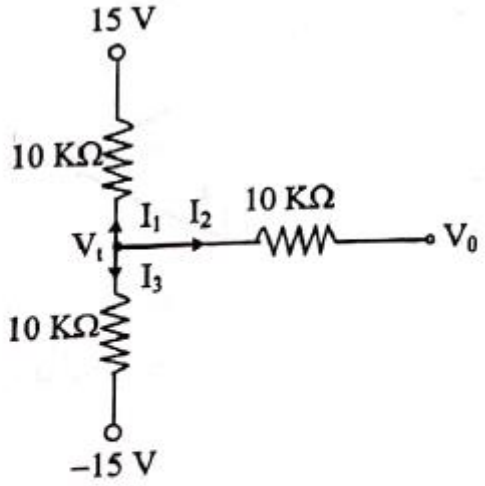
$$U_{tp} = 8V$$



Problems on Non-Linear Applications of Op-Amp

P04: A triangular wave which goes from -12V to +12V is applied to the inverting input of the Op-Amp Calculate the voltage that switches between the non-inverting input.





From KCL : $I_1 + I_2 + I_3 = 0$

$$\frac{V_t - 15}{10k} + \frac{V_t + 15}{10k} + \frac{V_t - V_0}{10k} = 0$$

$$3V_t = V_0$$

$$V_t = \frac{V_0}{3} \quad \ldots\ldots\ldots (1)$$

Threshold depends on output

So, when $V_0 = +15$

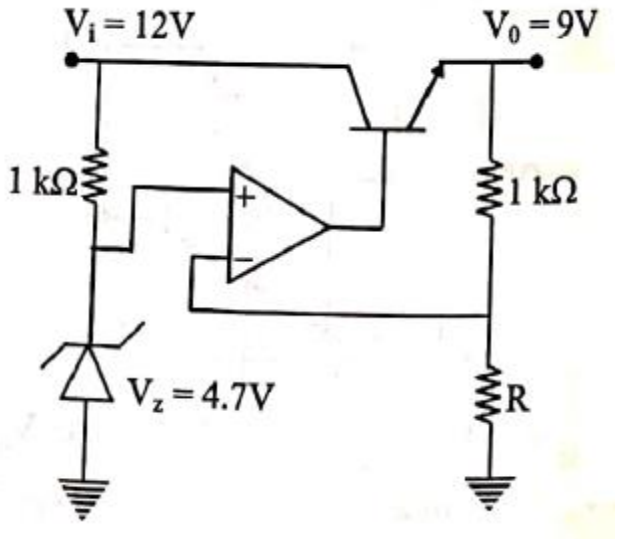
$$V_t = 15/3 = 5V.$$

When $V_0 = -15$

$$V_t = \frac{-15}{3} = -5V$$

Problems on Non-Linear Applications of Op-Amp

P05: In the voltage regulator circuit shown op-amp is ideal. BJT has V_{BE} = 0.7V and β=100 and the Zener voltage is 4.7V Calculate the value of R to have a regulated voltage of 9V



$$V^+ = V^- = 4.7V = V_R$$

Op-amp draws no current

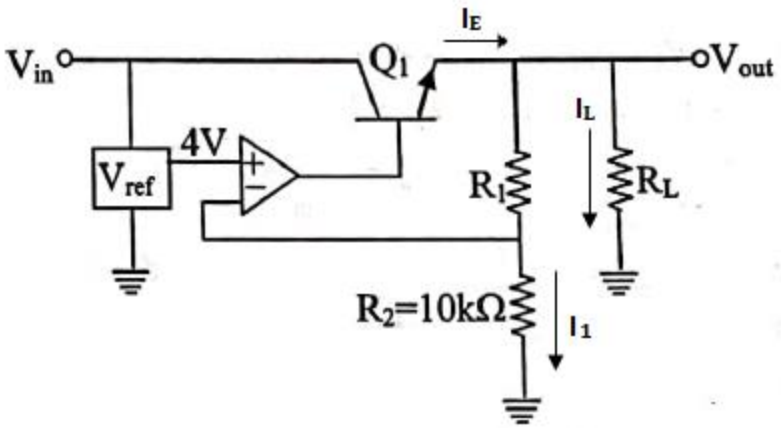
Hence $I_{1k\Omega} = I_R$

$$\frac{9 - 4.7}{1k} = \frac{4.7}{R}$$

$$R = 1093\ \Omega$$

Problems on Non-Linear Applications of Op-Amp

P06: Vin = 20V ± 20%, Vout = 10V, Calculate the maximum power dissipation in Q_1 if load current through R_L is 200mA



$$I_1 = \frac{4}{10k}$$

$$I_1 = 0.4 \text{ mA}$$

KCL at output node

$$I_E = I_1 + I_L$$

$$= 200 \text{ mA} + 0.4 \text{ mA}$$

$$I_E = 200.4 \text{ mA}$$

$$I_C \approx I_E = 200.4 \text{ mA}$$

It is given, $V_{in} = 20V \pm 20\%$

For maximum power dissipation

$$V_{in} = 20 + \frac{20 \times 20}{100}$$

$$V_{in} = 24V$$

$$V_{in} = V_C = 24V$$

$$V_E = V_0 = 10V$$

$$\therefore V_{CE} = V_C - V_E = 24 - 10 = 14 \text{ V}$$

∴ Maximum power dissipation

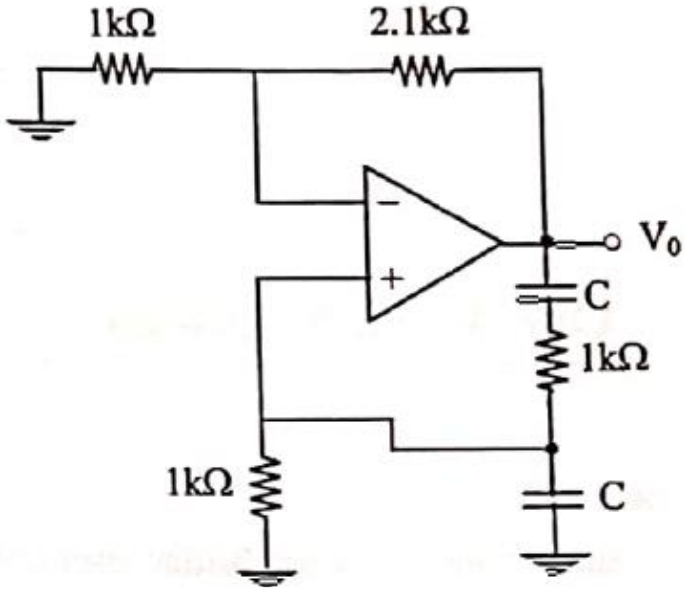
$$P_{max} = V_{CE} I_C$$

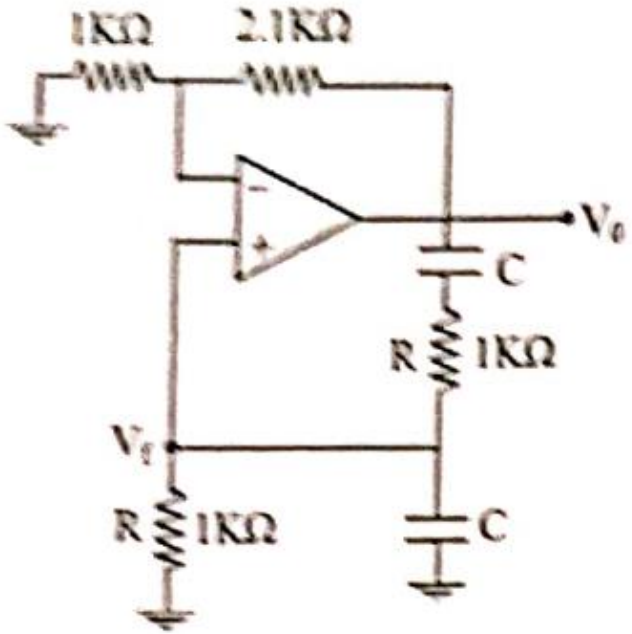
$$= 14 \times 200.4 \text{ m}$$

$$= 2.8056 \text{ W}$$

Problems on Non-Linear Applications of Op-Amp

P07: Calculate the value of C to have a sinusoidal frequency of 1kHz





$$\frac{V_0 - V_f}{R + X_C} = \frac{V_f}{R} + \frac{V_f}{X_C}$$

$$V_0 = (R + X_C)\frac{(R + X_C)V_f}{R.X_C} + V_f$$

$$\frac{V_f}{V_0} = \frac{R\,j\omega C}{R^2 - \frac{1}{\omega^2 C^2} + \frac{2R}{j\omega C} + \frac{R}{j\omega C}}$$

$$\frac{V_f}{V_0} = \frac{R}{J\omega CR^2 - \frac{j}{\omega C} + 3R}$$

For oscillators, imaginary part = 0

$$\omega CR^2 - \frac{1}{\omega C} = 0$$

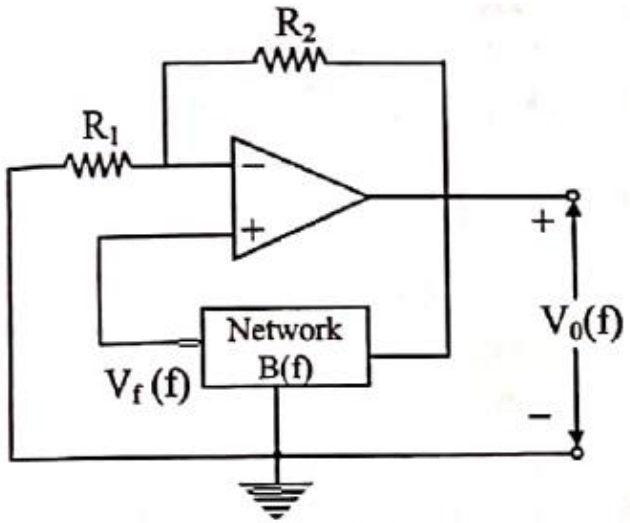
$$\Rightarrow C = \frac{1}{\omega R}$$

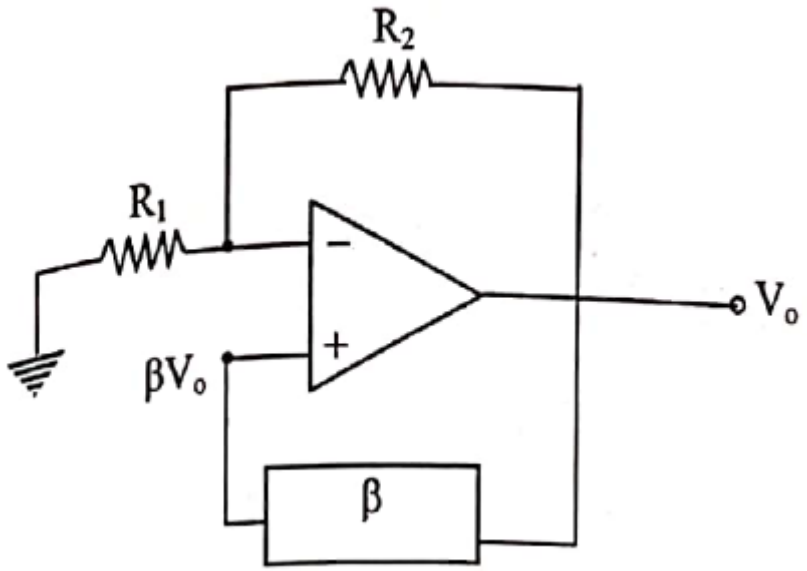
$$C = \frac{1}{2\pi \times 1 \times 10^3 \times 1 \times 10^3}$$

$$= \frac{1}{2\pi}\mu F$$

Problems on Non-Linear Applications of Op-Amp

P08: Calculate the ratio of R_2 to R_1 to have a sinusoidal frequency of fo kHz at $B(f) = \frac{V_f(f)}{V_0(f)} = \frac{1\angle 0}{6}$





$$\frac{\beta V_0 - 0}{R_1} + \frac{\beta V_0 - V_0}{R_2} = 0$$

$$\frac{\beta V_0}{R_1} + \frac{\beta V_0}{R_2} - \frac{V_0}{R_2} = 0$$

$$\beta V_0\left[\frac{1}{R_1} + \frac{1}{R_2}\right] = \frac{V_0}{R_2}$$

$$\beta\left[\frac{1}{R_1} + \frac{1}{R_2}\right] = \frac{1}{R_2}$$

$$\beta\left[\frac{R_2 + R_1}{R_1 R_2}\right] = \frac{1}{R_2}$$

$$\frac{R_1\left(1 + \frac{R_2}{R_1}\right)}{R_1} = \frac{1}{\beta}$$

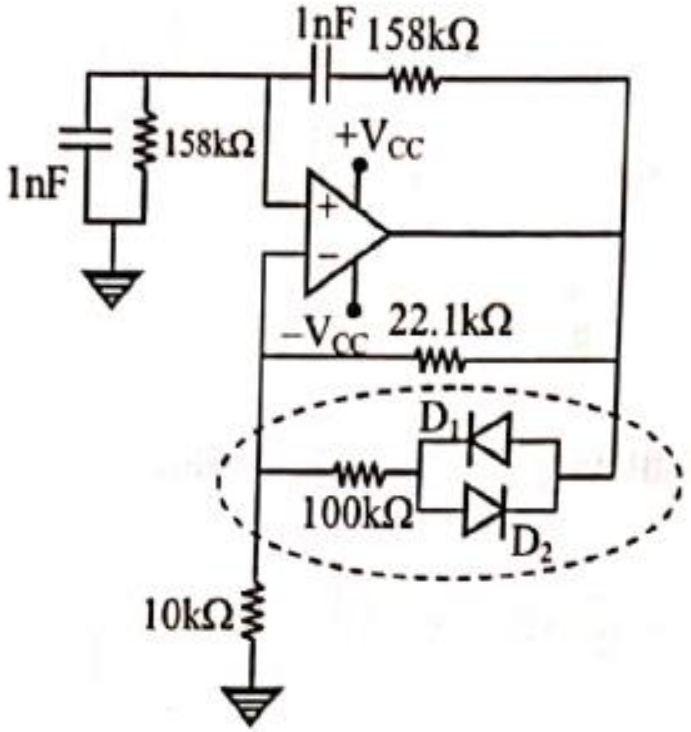
$$1 + \frac{R_2}{R_1} = \frac{1}{\beta}$$

Given $\frac{1}{\beta} = 6 \Rightarrow 1 + \frac{R_2}{R_1} = 6$

$$\frac{R_2}{R_1} = 5; \qquad R_2 = 5R_1$$

Problems on Non-Linear Applications of Op-Amp

P09: Identify the circuit and explain the function of 100KΩ resistor in series with two diodes connected back to back

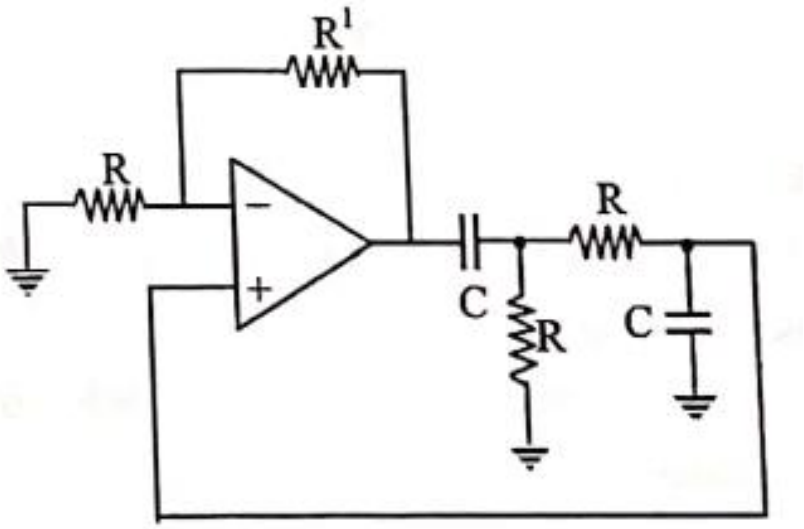


Ans:

- ***The circuit shown is a Wein Bridge Oscillator.***
- ***To provide amplitude stabilization by preventing the op-amp going into saturation. This will cause sinusoidal oscillations of fixed amplitude.***
- ***When oscillations grow, diodes conduct, D1—positive cycle D2—negative cycle.***
- ***22.1kΩ will come in parallel with 100kΩ, thereby reducing the effective resistance in the feedback.***
- ***Under equilibrium the loop gain will be unity.***

Problems on Non-Linear Applications of Op-Amp

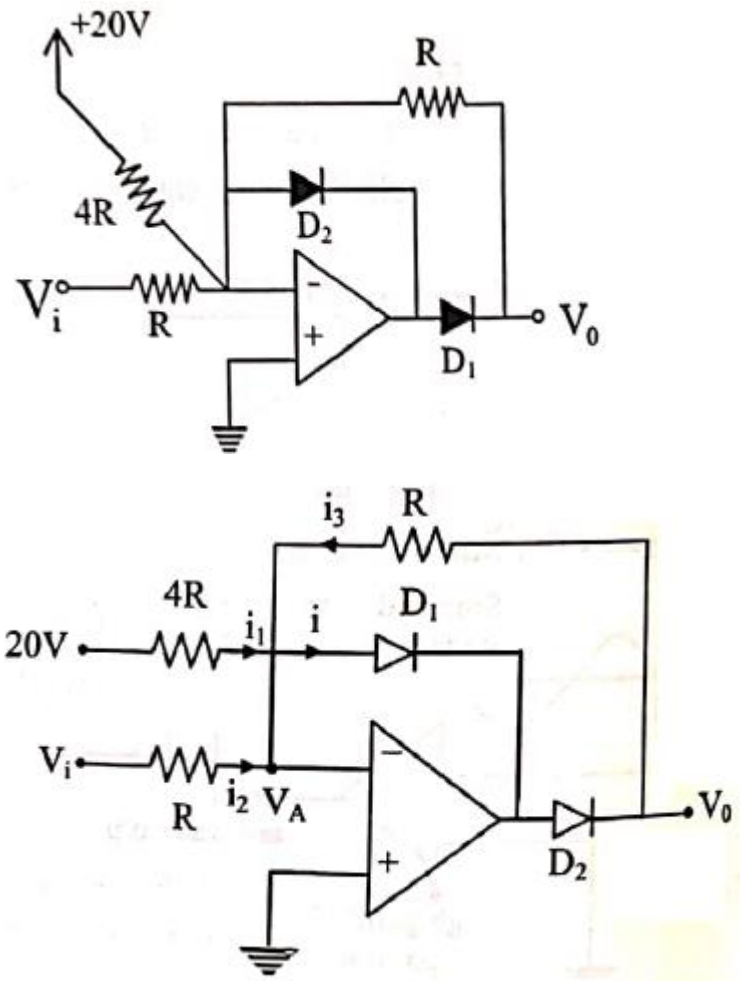
P10: Find the value of R^1 for generating sinusoidal oscillations. Also find the frequency of oscillations.



$$\textbf{Ans: } R^1 = 2R \quad and \quad \omega = \frac{1}{CR}$$

Problems on Non-Linear Applications of Op-Amp

P11: Plot the transfer characteristics of the Precision Rectifier circuit shown.



Case (1):

$$i_1 + i_2 + i_3 = i$$

$$\frac{20}{4R} + \frac{V_i}{R} + \frac{V_0}{R} = i$$

If V_0 is positive diode not conduct so $i = 0$.

Then $\frac{20}{4R} + \frac{V_i}{R} + \frac{V_0}{R} = 0$

$$5 + V_i + V_0 = 0$$

$$\therefore V_0 = -5 - V_i$$

At $V_i = -10V$

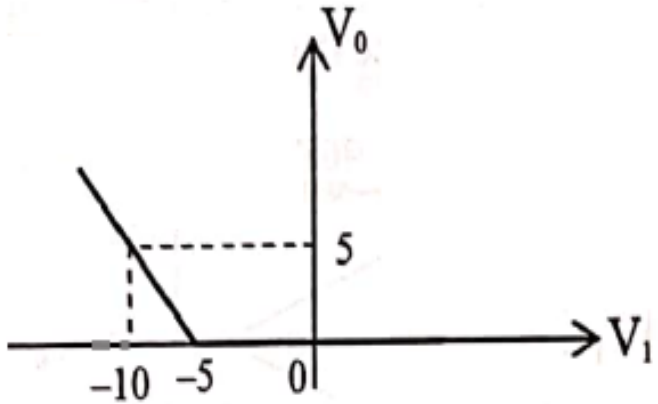
$V_0 = -5 + 10 = 5V$

At $V_i = -5V$

$V_0 = -5 + 5 = 0V$

When $V_i > -5V$, D_1 – OFF, D_2 – ON are conducting

so, $V_0 = 0V$.



Thank you