NOTE: Explanation Refer Class Notes

Analysis of Sequential Circuits

by
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Analysis of Sequential Circuit
(Planned Hours:10hours)

Lesson Schedule:

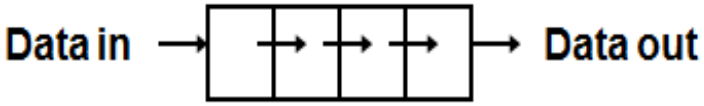
1. Registers
2. Registers
3. Counters
4. Binary Ripple Counters
5. Synchronous Binary counters
6. Ring and Johnson Counters
7. Design of a Synchronous counters
8. Design of a Synchronous Mod-n Counter using clocked JK
9. Design of a Synchronous Mod-n Counter using clocked D Flip-Flops
10. Design of a Synchronous Mod-n Counter using clocked T and SR Flip-Flops.

The Registers

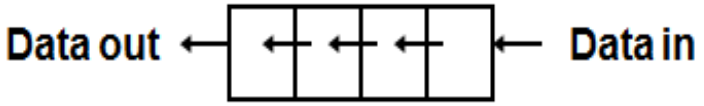
- Register – a collection of binary storage elements
- In theory, a register is sequential logic which can be defined by a state table
- More often, think of a register as storing a vector of binary values
- Frequently used to perform simple data storage and data movement and processing operations

Shift Registers

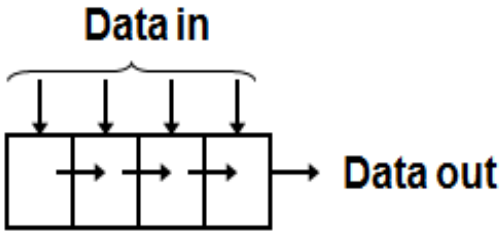
A Shift Register is a sequential logic device made up of flip-flops that allows parallel or serial loading and serial or parallel outputs as well as shifting bit by bit.



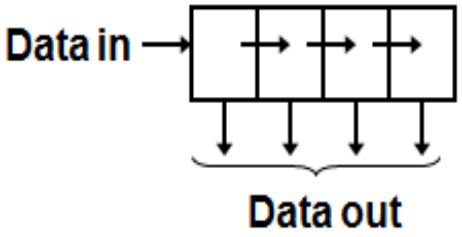
(a) Serial in/shift right/serial out



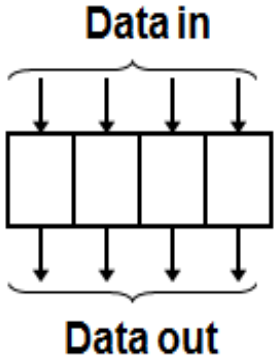
(b) Serial in/shift left/serial out



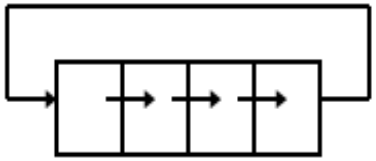
(c) Parallel in/serial out



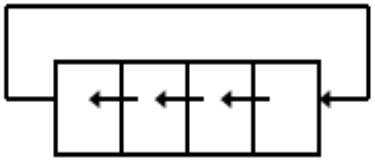
(d) Serial in/parallel out



(e) Parallel in / parallel out



(f) Rotate right



(g) Rotate left

SHIFT REGISTER VOCABULARY

REGISTER- group of flip flops capable of storing data.

SERIAL DATA TRANSMISSION- transfer of data from one place to another one bit at a time.

PARALLEL DATA TRANSMISSION- simultaneous transfer of all bits of a data word from one place to another.

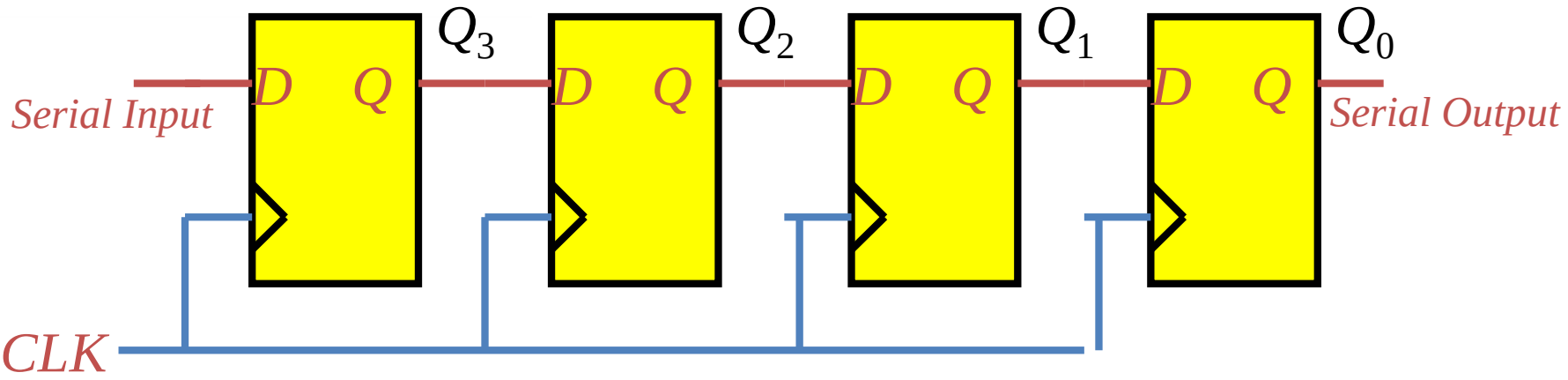
SISO- SERIAL IN/SERIAL OUT- type of register that can be loaded with data serially and has only one serial output.

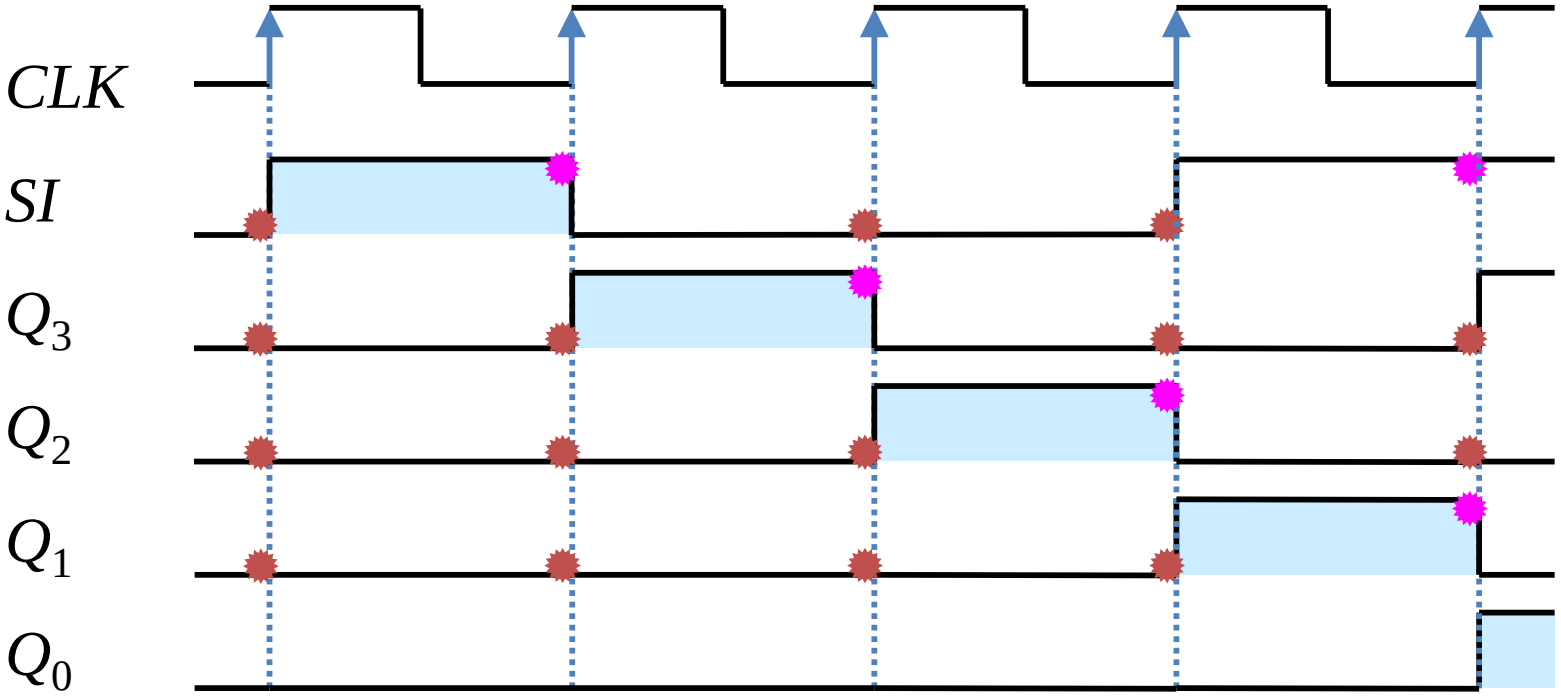
SIPO- SERIAL IN/PARALLEL OUT- type of register that can be loaded with data serially and has parallel outputs available.

PISO- PARALLEL IN/SERIAL OUT- type of register that can be loaded with parallel data and has only one serial output.

PIPO- PARALLEL IN/PARALLEL OUT- type of register that can be loaded with parallel data and has parallel outputs available.

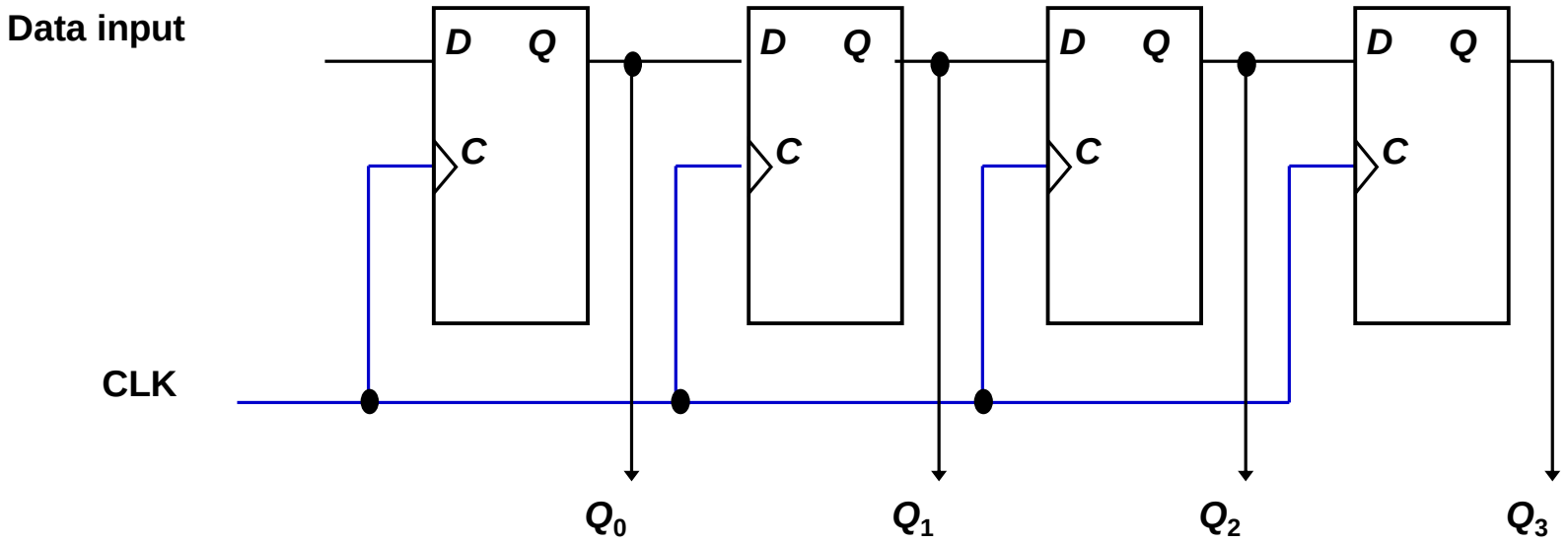
Serial in Serial out (SISO)





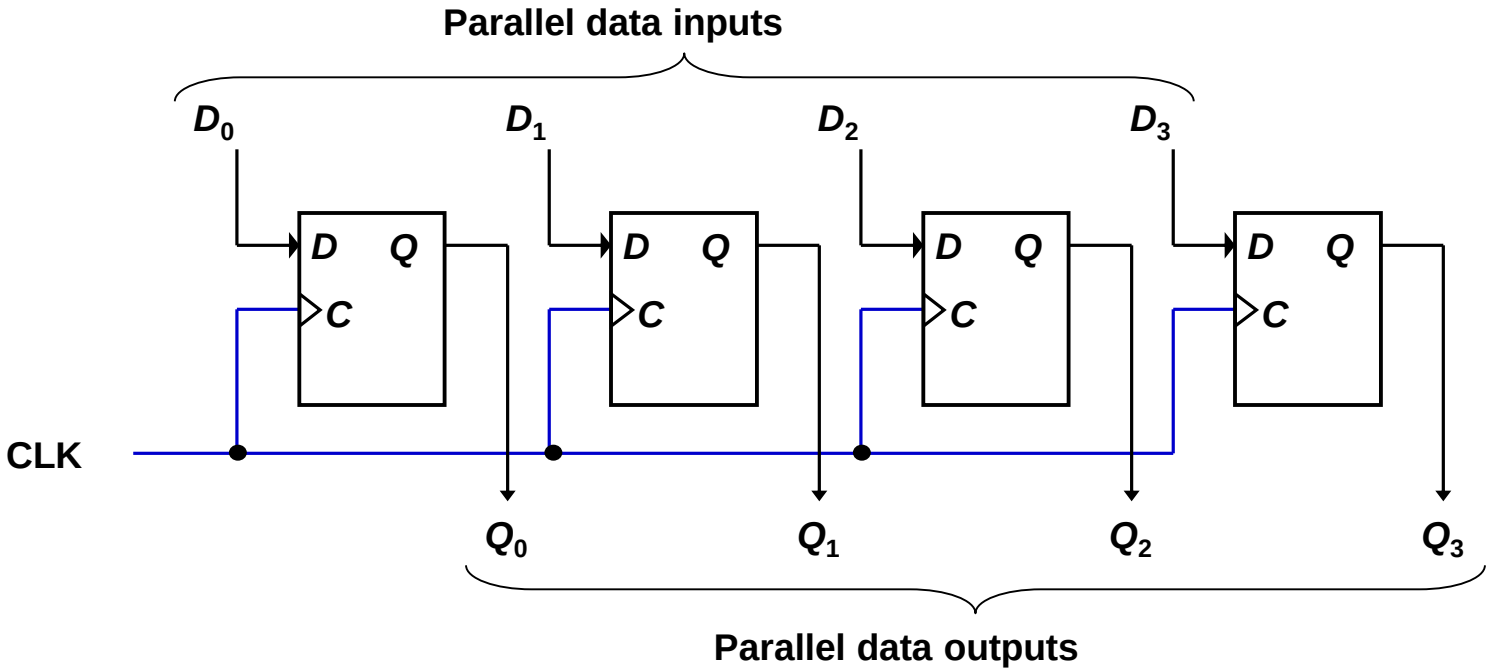
Serial In Parallel Out(SIPO)

- Accepts data serially.
- Outputs of all stages are available simultaneously.



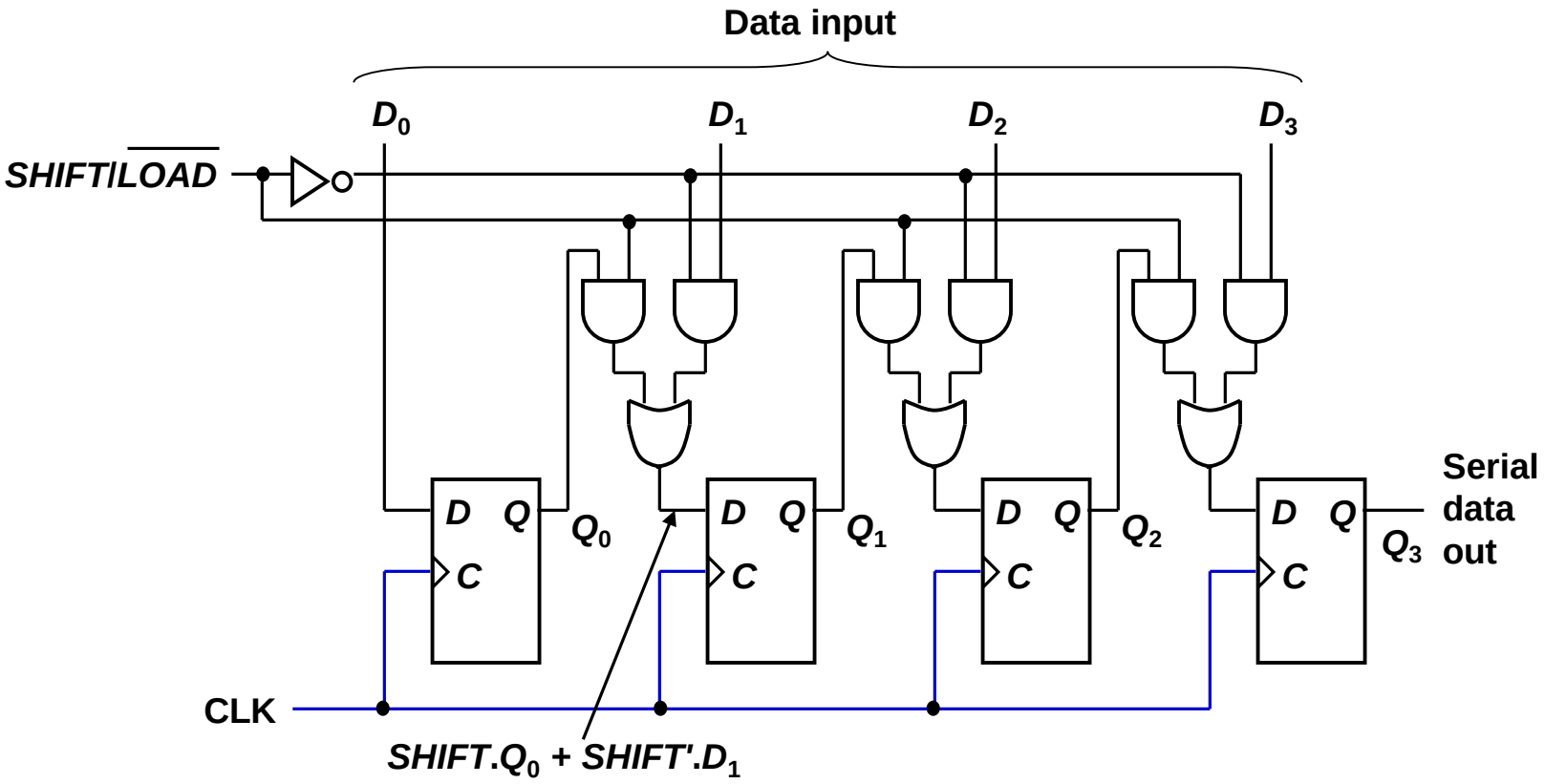
Parallel In Parallel Out (PIPO)

- Simultaneous input and output of all data bits.



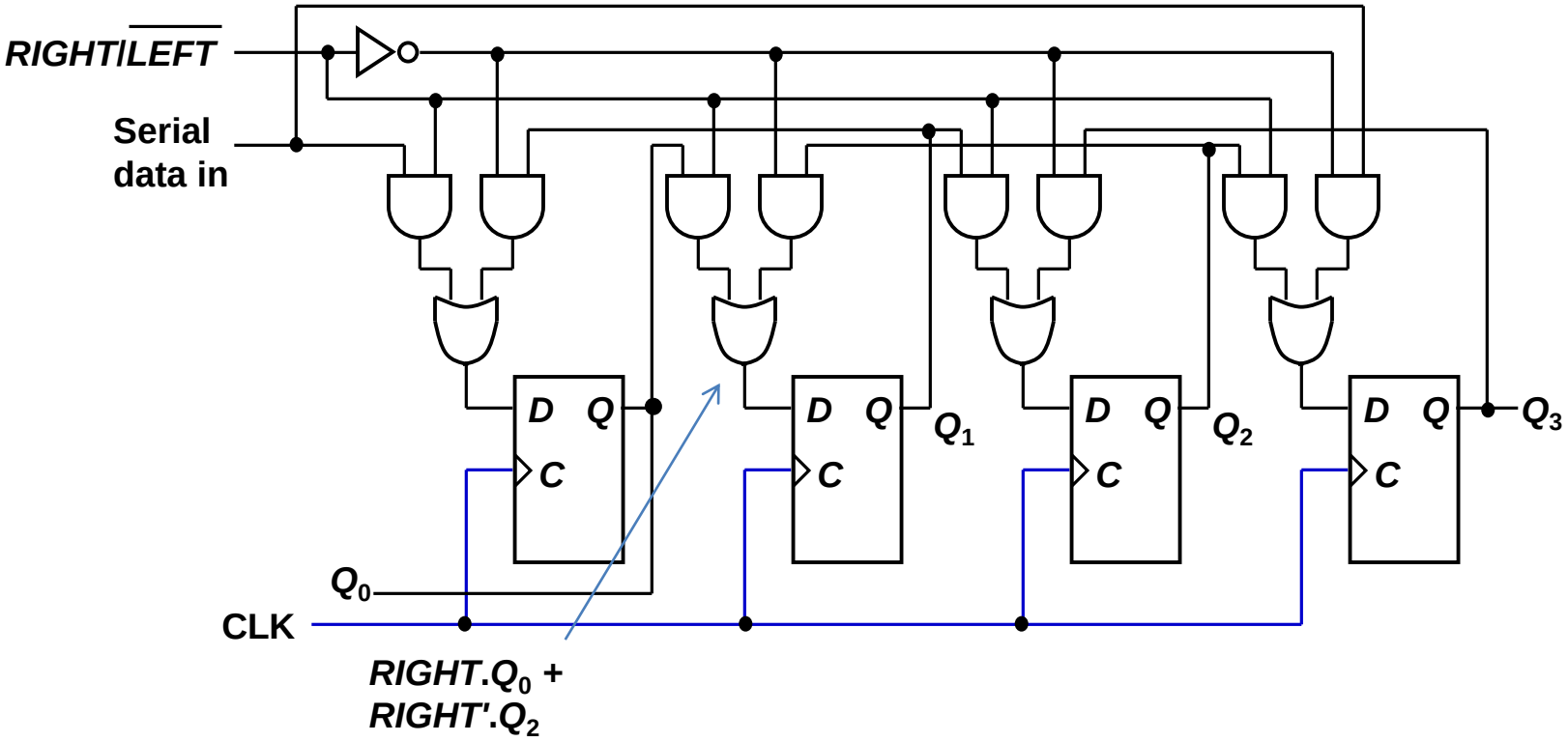
Parallel In Serial Out (PISO)

- Bits are entered simultaneously, but output is serial.



Bidirectional Shift Registers

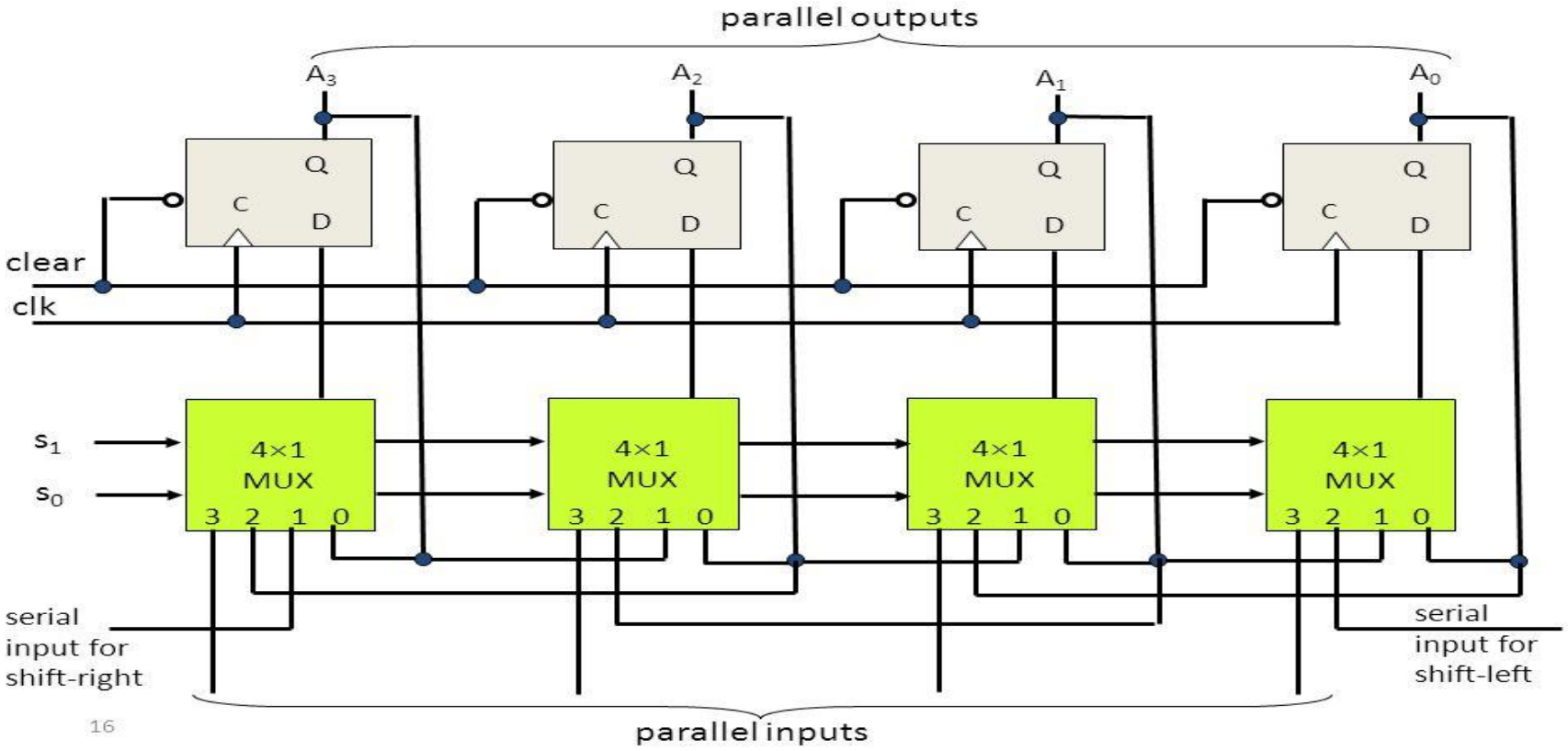
- Data can be shifted either left or right, using a control line RIGHT/LEFT (or simply RIGHT) to indicate the direction.



Universal Shift Register

- 4-bit bidirectional shift register with parallel load.

Mode Select		Register Operation
S1	S0	
0	0	Hold
0	1	Shift right
1	0	Shift left
1	1	Parallel load



Shift Register Counters

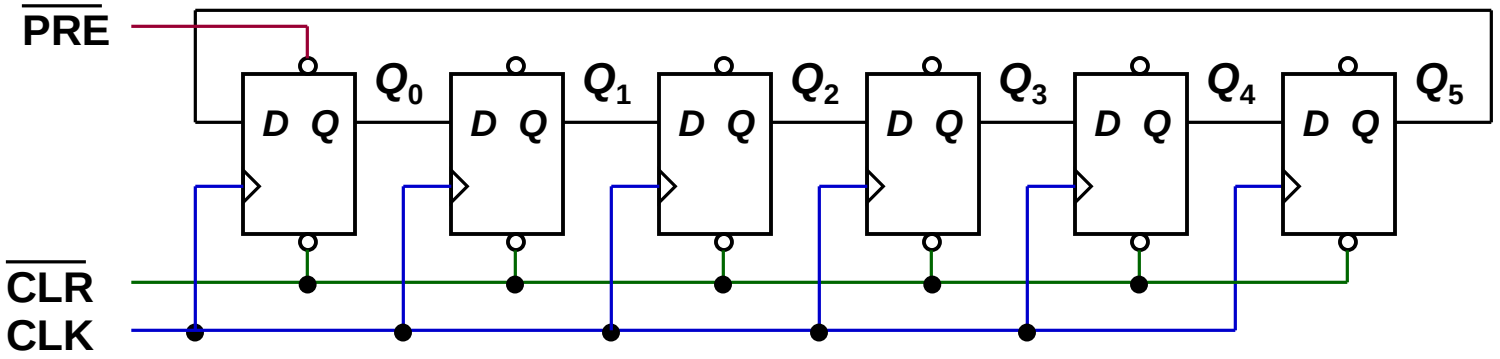
- Shift register counter: a shift register with the serial output connected back to the serial input.
- They are classified as counters because they give a specified sequence of states.
- Two common types: the *Johnson counter* and the *Ring counter*.

Ring Counters

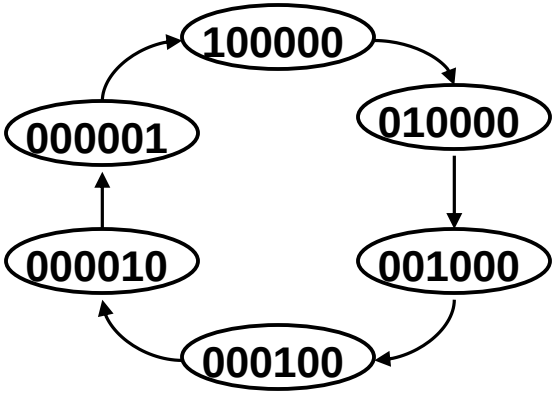
- One flip-flop (stage) for each state in the sequence.
- The output of the last stage is connected to the D input of the first stage.
- An n-bit ring counter cycles through n states.
- No decoding gates are required, as there is an output that corresponds to every state the counter is in.

Ring Counters

- Example: A 6-bit ring counter.



Clock	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5
→0	1	0	0	0	0	0
1	0	1	0	0	0	0
2	0	0	1	0	0	0
3	0	0	0	1	0	0
4	0	0	0	0	1	0
5	0	0	0	0	0	1

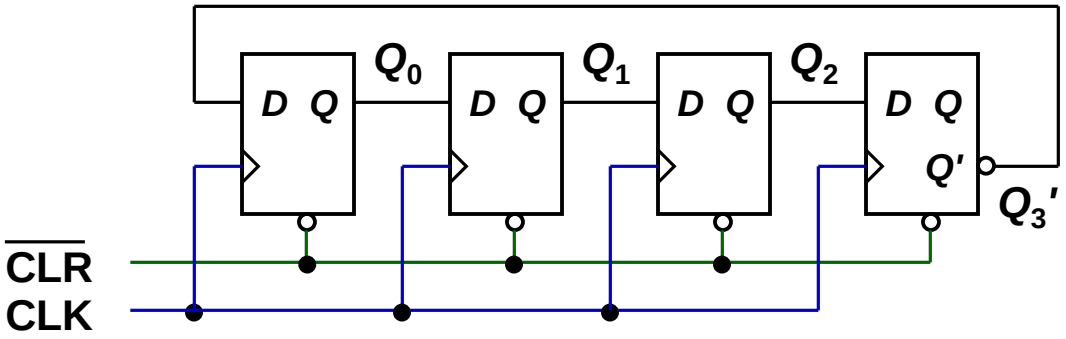


Johnson Counters

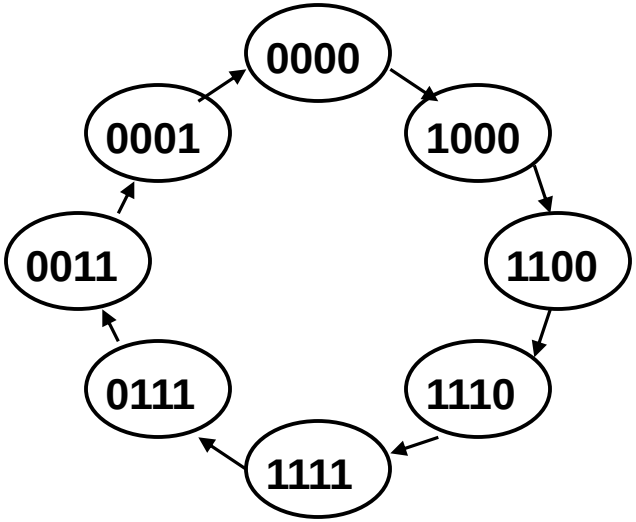
- The complement of the output of the last stage is connected back to the D input of the first stage.
- Also called the *twisted-ring counter*.
- Require fewer flip-flops than ring counters but more flip-flops than binary counters.
- An *n*-bit Johnson counter cycles through 2*n* states.
- Require more decoding circuitry than ring counter but less than binary counters.

Johnson Counters

- Example: A 4-bit Johnson counter.



Clock	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1



Introduction: Counters

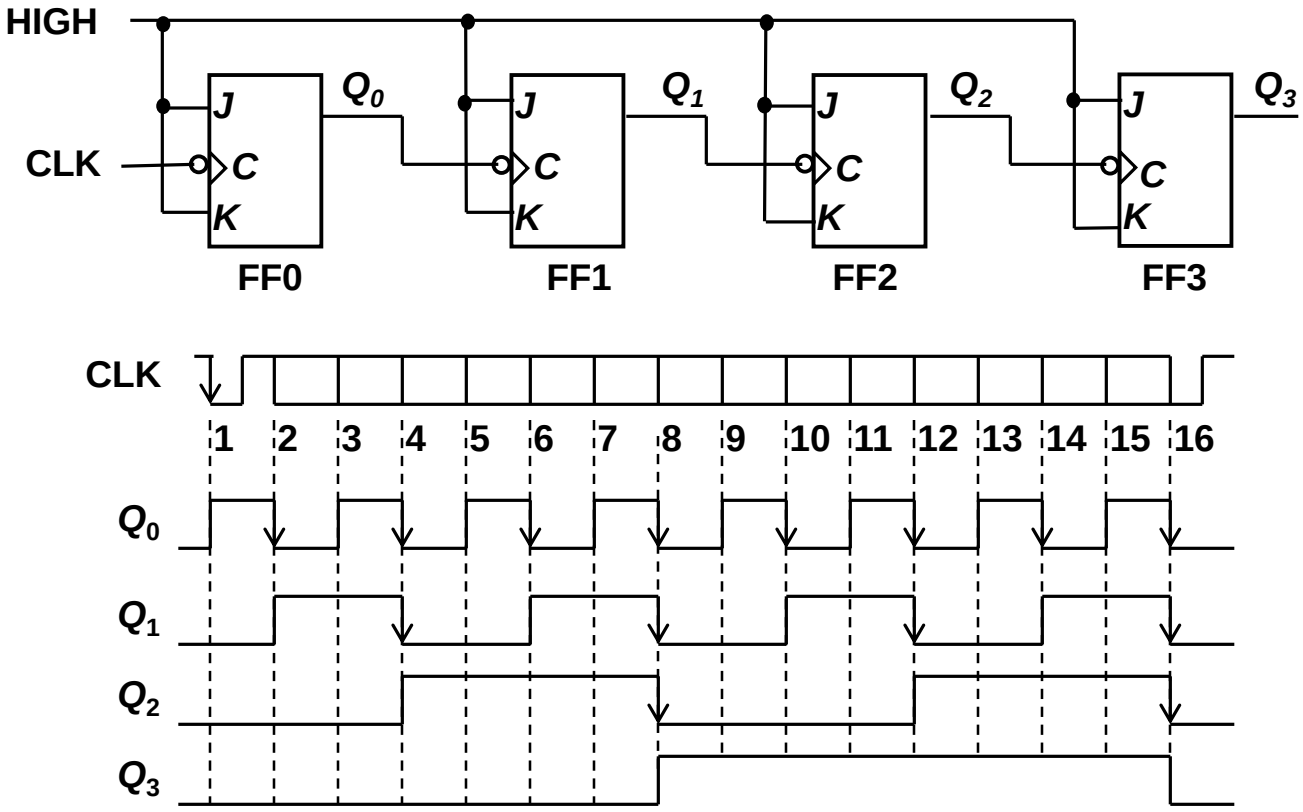
- Counters are circuits that cycle through a specified number of states.
- Two types of counters:
  - synchronous (parallel) counters
  - asynchronous (ripple) counters
- Ripple counters allow some flip-flop outputs to be used as a source of clock for other flip-flops.
- Synchronous counters apply the same clock to all flip-flops.

Asynchronous (Ripple) Counters

- Asynchronous counters: the flip-flops do not change states at exactly the same time as they do not have a common clock pulse.
- Also known as ripple counters, as the input clock pulse "ripples" through the counter – cumulative delay is a drawback.
- *n* flip-flops $\rightarrow$ a MOD (modulus) 2^n counter. (Note: A MOD-*x* counter cycles through *x* states.)
- Output of the last flip-flop (MSB) divides the input clock frequency by the MOD number of the counter, hence a counter is also a *frequency divider*.

Asynchronous (Ripple) Counters

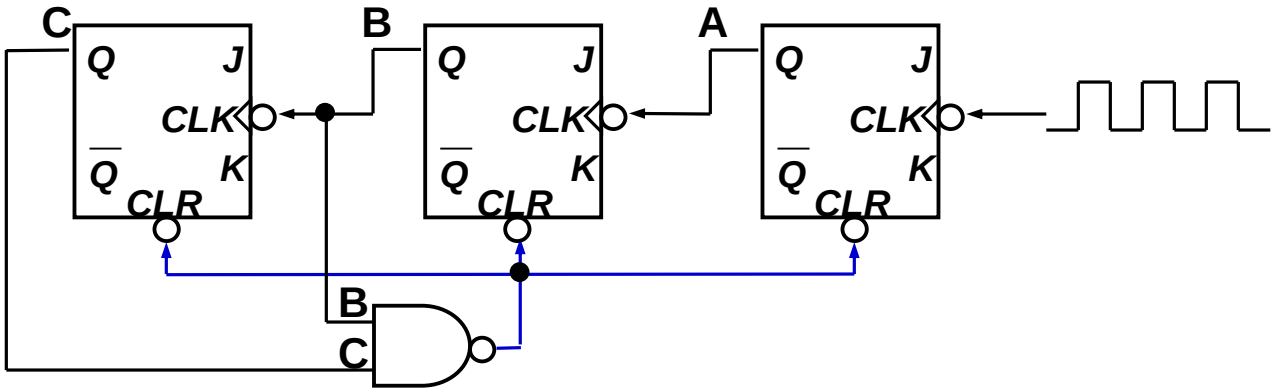
- Example: 4-bit ripple binary counter (negative-edge triggered).



Asyn. Counters with MOD no. < 2^n

- States may be skipped resulting in a truncated sequence.
- Technique: force counter to *recycle before going through all of the states* in the binary sequence.
- Example: Given the following circuit, determine the counting sequence (and hence the modulus no.)

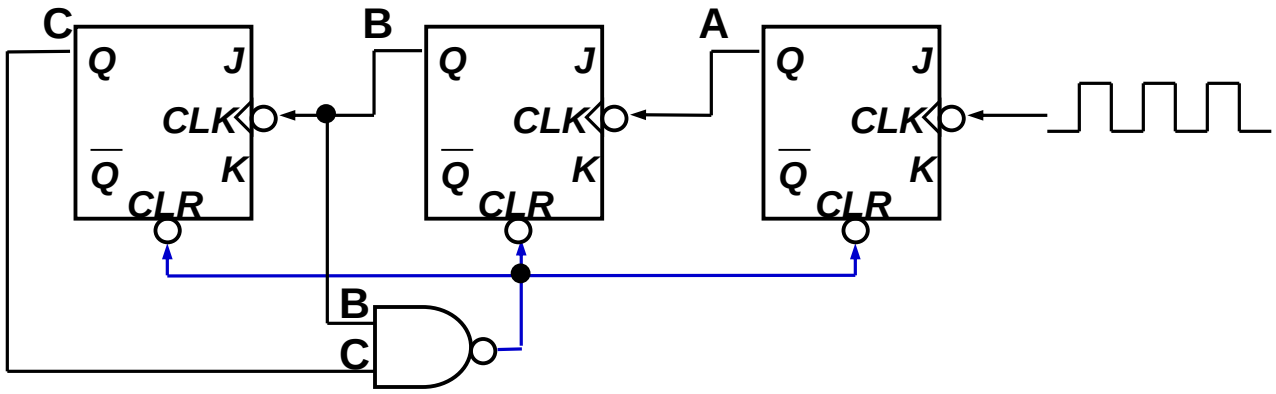
All *J*, *K* inputs are 1 (HIGH).

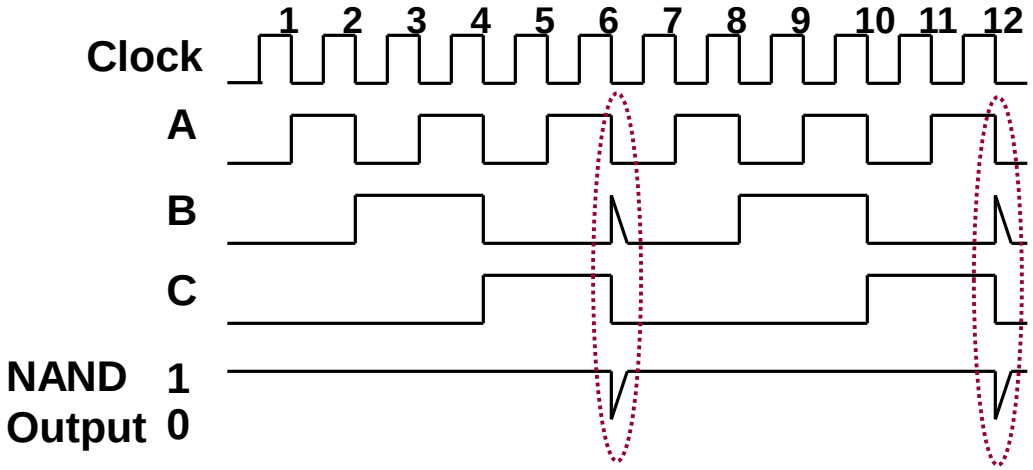


Asyn. Counters with MOD no. < 2^n

- Example (cont'd):

All *J*, *K* inputs are 1 (HIGH).

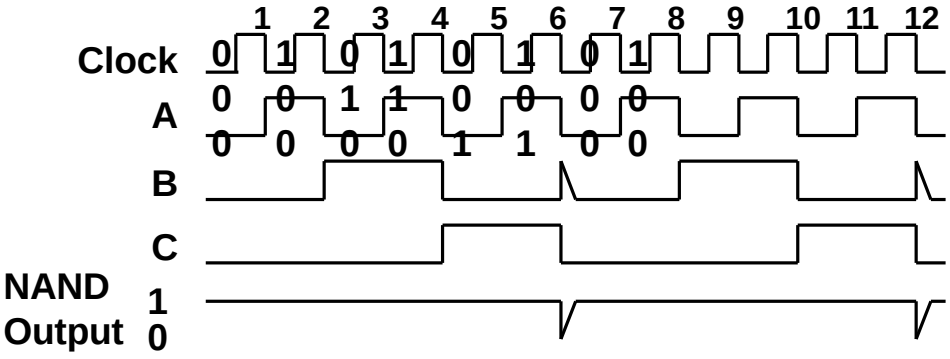


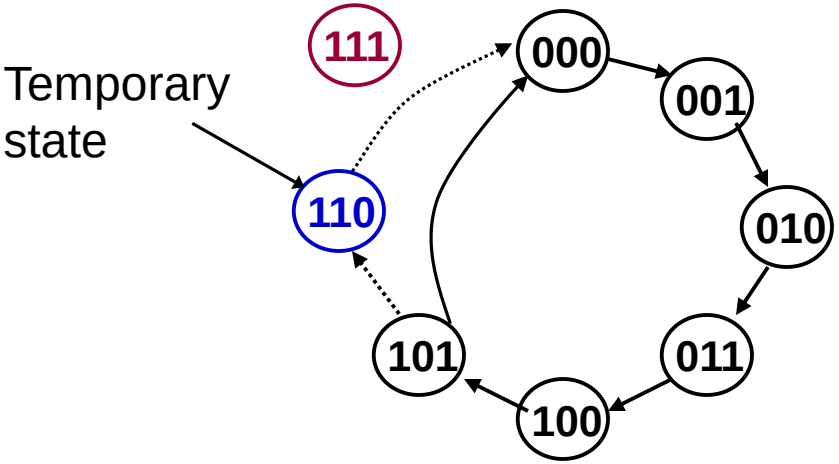


MOD-6 counter produced by clearing (a MOD-8 binary counter) when count of six (110) occurs.

Asyn. Counters with MOD no. < 2^n

- Example (cont'd): Counting sequence of circuit (in CBA order).

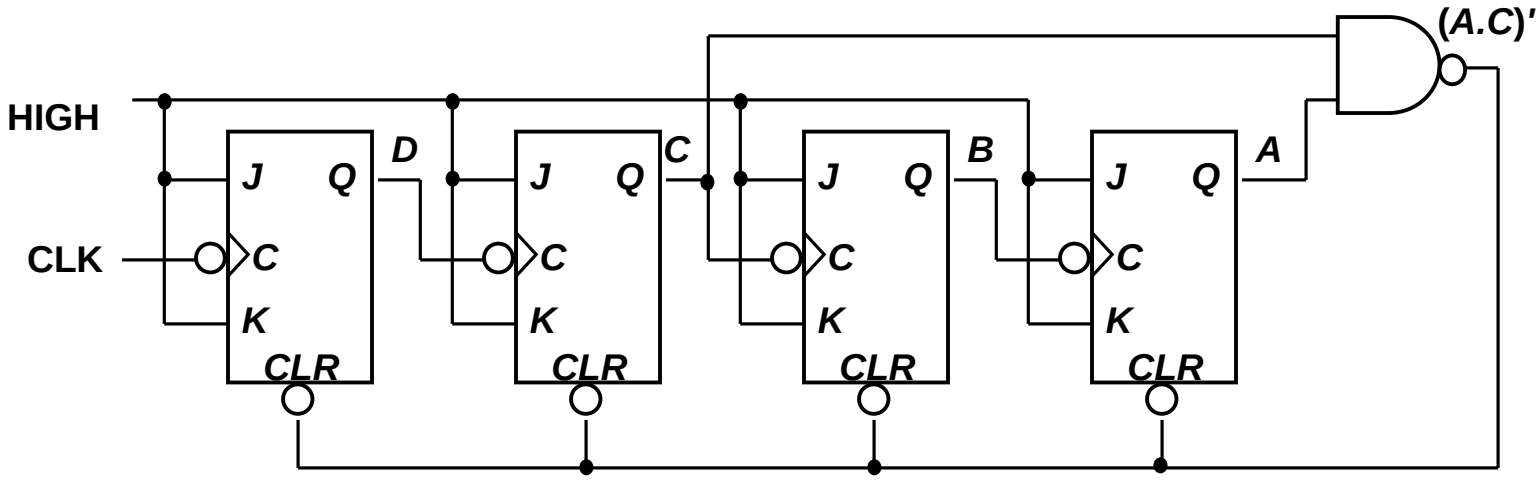




Counter is a MOD-6 counter.

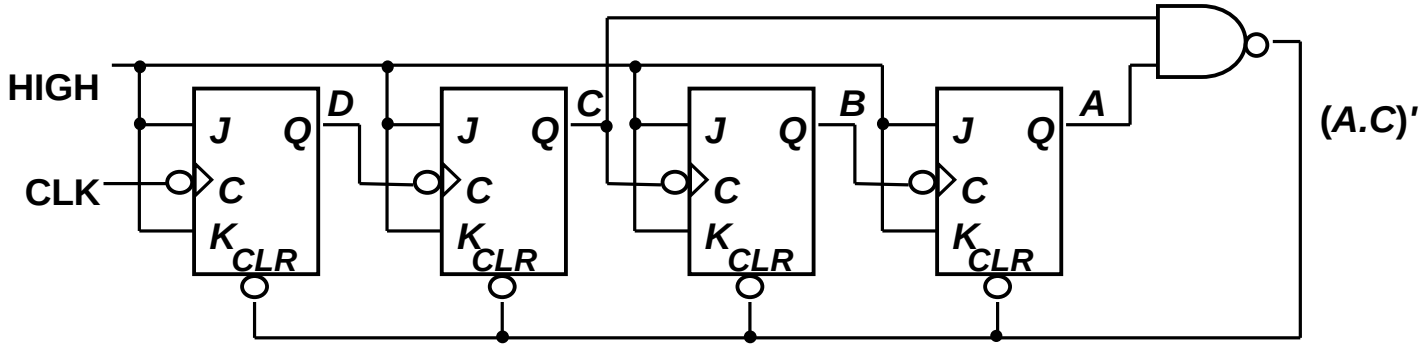
Asyn. Counters with MOD no. < 2^n

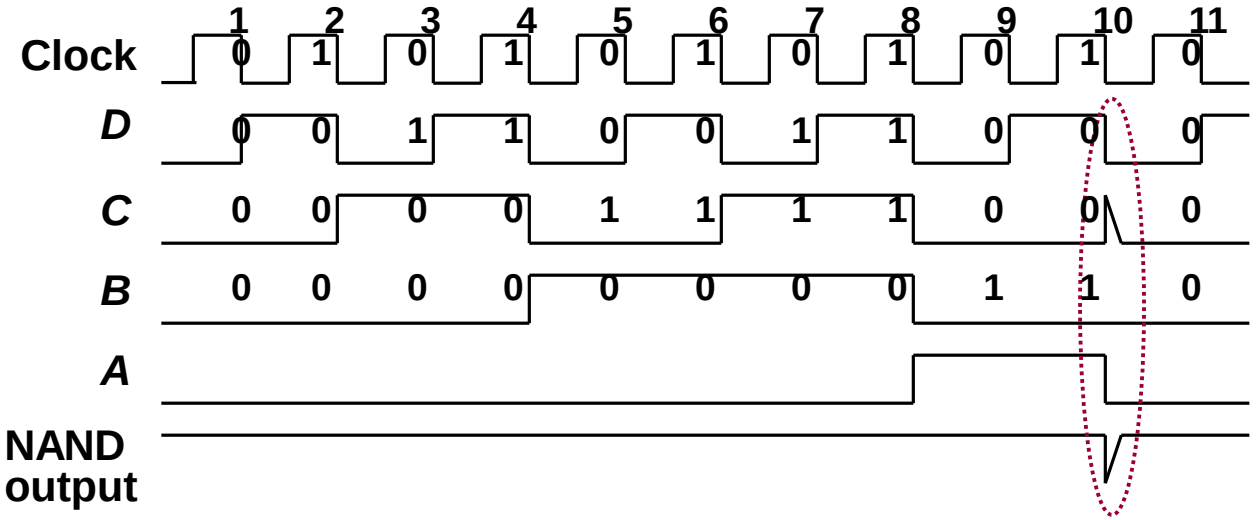
- Decade counters (or BCD counters) are counters with 10 states (modulus-10) in their sequence. They are commonly used in daily life (e.g.: utility meters, odometers, etc.).
- Design an asynchronous decade counter.



Asyn. Counters with MOD no. < 2^n

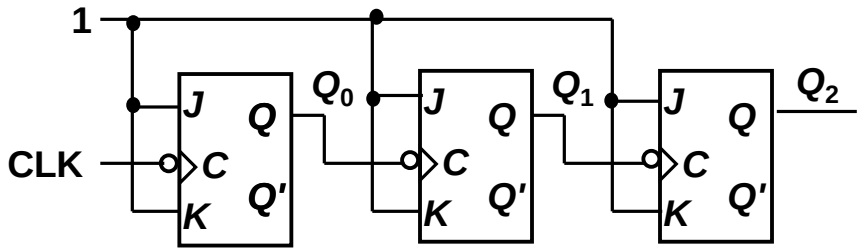
- Asynchronous decade/BCD counter (cont'd).



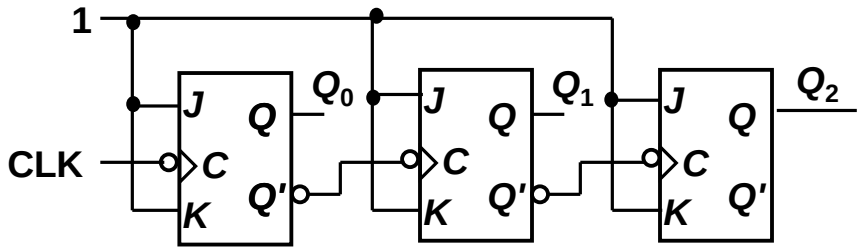


Asynchronous Down Counters

- So far we are dealing with *up counters*. *Down counters*, on the other hand, count downward from a maximum value to zero, and repeat.
- Example: A 3-bit binary (MOD-2^3) down counter.



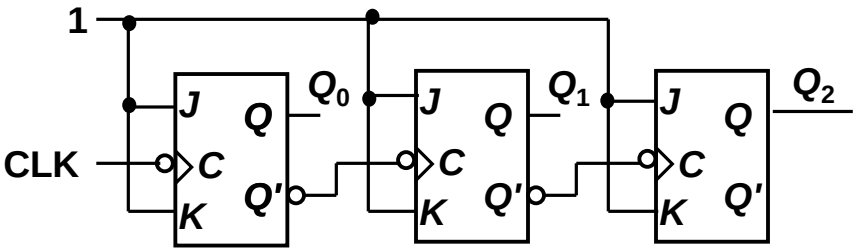
3-bit binary up counter

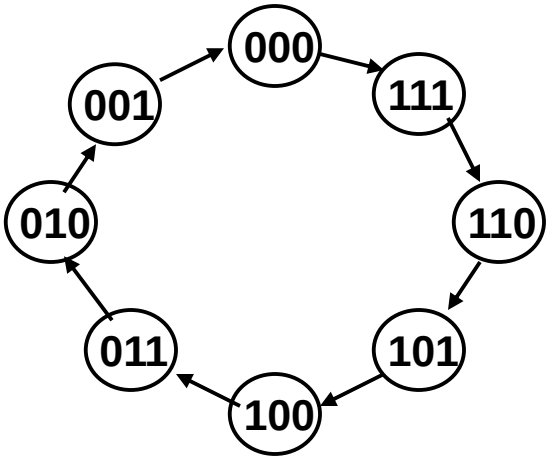


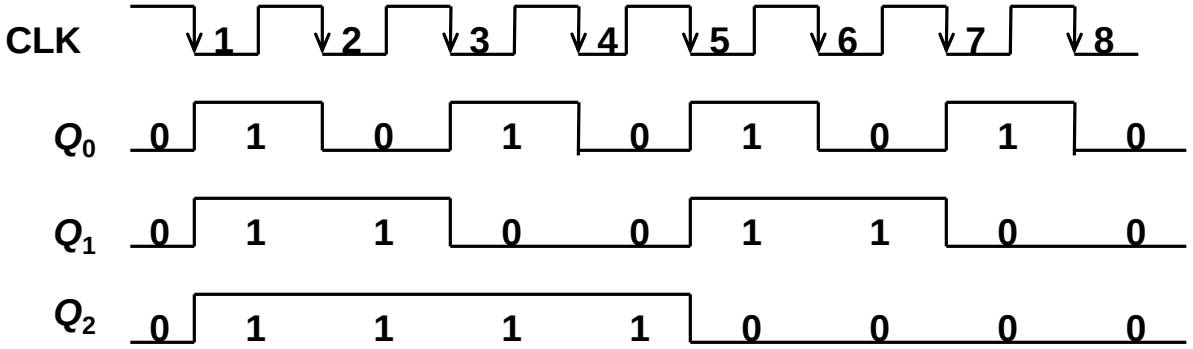
3-bit binary down counter

Asynchronous Down Counters

- Example: A 3-bit binary (MOD-8) down counter.

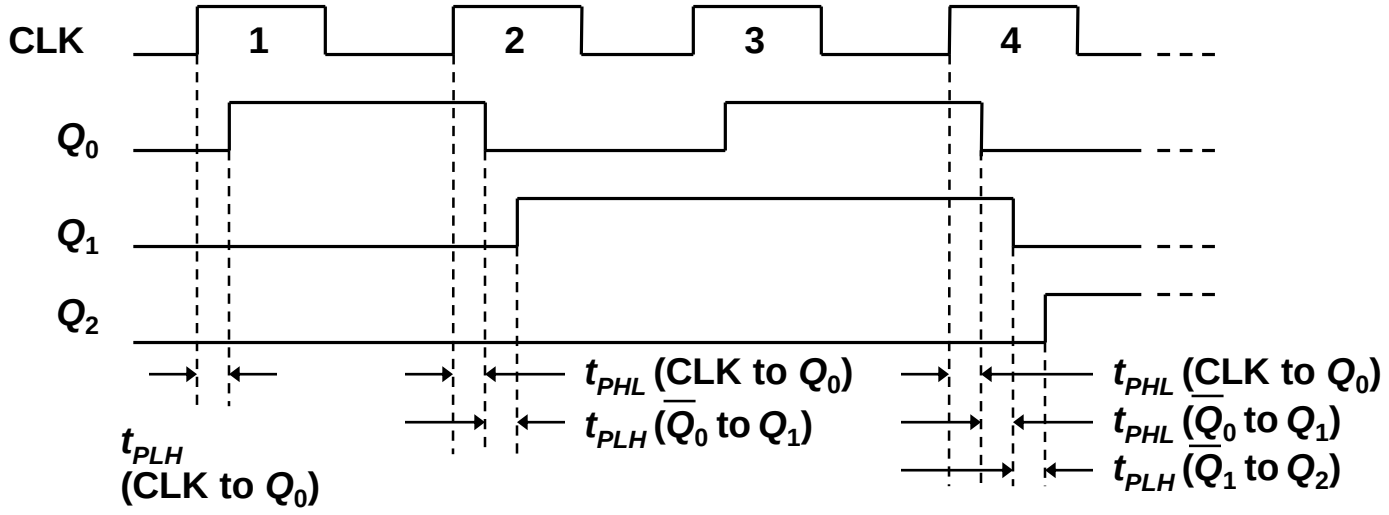






Asynchronous (Ripple) Counters

- Propagation delays in an asynchronous (ripple-clocked) binary counter.
- If the accumulated delay is greater than the clock pulse, some counter states may be misrepresented!



Design of a Synchronous Mod-n Counter using clocked JK Flip-Flops

REFER THE CLASS NOTES

Design of a Synchronous Mod-n Counter using clocked T Flip-Flops

REFER THE CLASS NOTES

Design of a Synchronous Mod-n Counter using clocked D Flip-Flops

REFER THE CLASS NOTES

Design of a Synchronous Mod-n Counter using clocked SR Flip-Flops

REFER THE CLASS NOTES

Design of a Synchronous Counter using clocked SR Flip-Flops

Sequence = 0 – 1 – 3 – 4 – 2 – 0

REFER THE CLASS NOTES