USN

III Semester B.E. Examination
(Electronics and Communication Engineering)
Digital Circuits (ECC235)

Duration: 3 hours **Max. Marks: 100**

Note: *i) Answer any TWO full questions from UNIT-I, any TWO full questions from UNIT-II and any ONE full question from UNIT-JII.*

UNIT-I

1 a. With the help of neat circuit diagram explain the working of a two input TTL NAND gate. (06 marks)

b. Simplify the given boolean function by using K-map method and express it in SOP form. Realize the logic circuit by using NAND gates only.

$f(A,B,C,D)= \Sigma m(7,9,10,11,12,13,14,15)$ (06 marks)

c. With truth table and expression, implement the 8:3 priority encoder where highest priority is given to MSB bit. (08 marks)

2 a. With the help of neat circuit diagram explain the working of a MOS inverter. (06 marks)

b. What is magnitude comparator? Write the truth table and circuit diagram of 1 bit comparator. (06 marks)

c. Find the prime implicants for boolean expression by using Quine McClusky method.

$f(A,B,C,D)= \Sigma m(1,3,6,7,8,9,10,12,14,15)+d(11,13)$ (08 marks)

3 a. With the help of neat circuit diagram explain the working of a ECL OR gate. (06 marks)

b. Simplify the given boolean function by using K-map method in POS form.

$f(A,B,C,D)= \Sigma m(0,1,2,3,4,5,7)$ (06 marks)

c. Design a decimal adder using IC 7483. (08 marks)

UNIT-II

4 a. Explain the operation of SR latch using NOR gates. (06 marks)

b. Find the characteristic equations of JK FF and D FF. (06 marks)

c. Explain the four basic types of shift registers with neat block diagram. (08 marks)

5 a. Explain the operation of a simple SR FF for switch debouncer application. (06 marks)

b. Compare the ripple and synchronous counters. (06 marks)

c. Design a mod-5 asynchronous counter with initial state $(001)_2$ and draw the timing diagram. (08 marks)

6 a. Explain the working of JK FF. Write its truth table and excitation table. What is race around condition? (10marks)

b. Design mod-6 synchronous counter by using SR FF. (10marks)

UNIT-III

7 a. Write a note on Moore and mealy model with respect to design of sequential circuits. Compare the two models. (06 marks)

b. Draw an ASM chart for a 2 bit counter having one enable line E such that E=1 (count enable) & E=0 (count disable) (06 marks)

c. Explian the following terms, transition equation, transition table, excitation table, state table (08 marks)

8 a. Design a synchronous circuit that has a single input variable and single output variable. The input data are received serially. Cause the first output bit to be the same value as the first input bit in the serial string (i.e. if x=0, then z=0; if x=1 then z=1). Output z is to change thereafter only when three consecutive input bits have the same value for example, (10marks)

x= 00100111011000 , z=00000001111110

Construct ASM, state table and realize the design using JK FF.

b. Write note on following, (10marks)

i) state reduction using equivalence classes

ii) state reduction using implication charts

Set	1	2	3
(Tick √ appropriately)			

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Scheme & Solutions

- **A scheme & solution does not mean the splitting of final marks allocated into its component parts (example 2+2+4+2). It has to clearly show the detailed expected answers / response for each component.**

Exam: B.E. / B.Arch. / M. Tech./M.C.A./M.B.A./Ph.D Academic Program ...BE.....Sem.: III

Course: Digital Circuits

Course Code: ECC235 Duration of Paper: 3 Hrs. Maximum marks: 100

Question Number	Solution	Marks Allocated
	Unit-I	
1.a.	Circuit diagram of TTL NAND gate - 3M and explanation of its working - 3M	6M
1.b.	Simplification - 4M Logic diagram - 2M Expression from K-map ; $f = AB + \bar{A}D + \bar{A}C + BC\bar{D}$ " for NAND realization, $f = \overline{AB} \cdot \overline{\bar{A}D} \cdot \overline{\bar{A}C} \cdot \overline{BC\bar{D}}$	6M
1.c.	For truth table - 2M Simplification of expression - 3M For logic diagram - 3M	8M
2.a.	Circuit diagram of MOS inverter - 3M and explanation of its working - 3M	6M
2.b.	Comparator definition - 2M Truth table and simplification of expression - 2M Logic diagram - 2M	6M

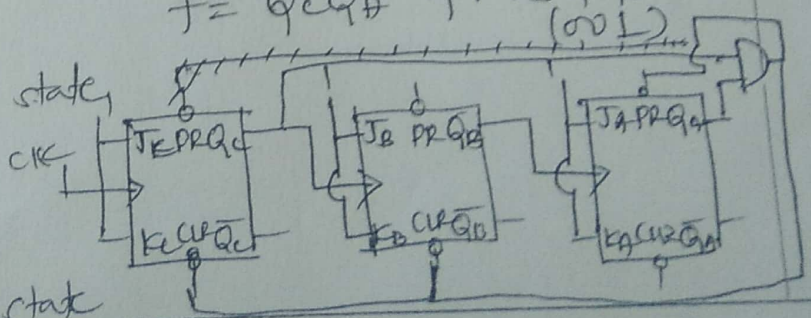
Question Number	Solution	Marks Allocated
2.c.	Using Q-M method, 1st level grouping - 3M 2nd " " - 2M 3" " " - 2M Final prime implicants - 1M → P = A, Q = BC, R = CD, S = $\bar{B}D$	8M
3.a.	Circuit diagram of ECL OR gate - 3M and explanation of operation - 3M	6M
3.b.	$f(A,B,C,D) = \Sigma m(0,1,2,3,4,5,7)$ K-map: CD: 00 01 11 10; AB: 00 01 11 10 00: 1 1 1 1 01: 1 1 1 1 11: 0 0 0 0 10: 0 0 0 0 $f = (\bar{A}).(\bar{B}+\bar{C}+D)$ For K-map and grouping - 3M For simplified expression - 3M	6M
3.c.	For truth table - 2M For simplification - 3M For logic diagram - 3M	8M
	Unit - II	
4.a.	For logic diagram of SR latch - 2M and explanation of operation with truth table - 4M	6M

Question Number	Solution	Marks Allocated
4.b.	Characteristic equation of JK FF – 3M " " D FF – 3M	6M
4.c.	Explanation of following shift register with diagram Serial in serial out shift reg. – 2M " Parallel " " " – 2M Parallel in serial " " " – 2M " " parallel out " " – 2M	8M
5.a.	For Circuit diagram – 2M and explanation of operation with timing diagram – 4M	6M
5.b.	Differences between Ripple and Synchronous Counters.	6M
5.c.	For truth table – 2M, Simplified expression – 2M For logic diagram – 4M	8M

Truth table

Q_C	Q_B	Q_A	
0	0	1	← Initial state
0	1	0	
0	1	1	
1	0	0	
1	0	1	← Final state

$f = Q_C Q_B$ for reset to (001)



└ unique combination

Question Number	Solution	Marks Allocated
6.a.	Truth table – 1M Excitation table – 1M logic ~~Block~~ diagram of JK FF – 2M and explanation of operation – 4M explanation of Race around condition – 2M	10M
6.b.	Excitation table of SR-FF – 2M State transition table – 3M For finding equations – 3M Final logic diagram – 2M	10M
	Unit – III	
7.a.	Moore model – 2M Mealy " – 2M Comparision of moore and mealy – 2M	6M
7.b.	Drawing ASM chart of 2 bit Counter – 3M & explanation of operation – 3M	6M
7.c.	Explanation of transition equation – 2M " " table – 2M " excitation " – 2M " state " – 2M	8M

8.a. ASM diagram — 3M

State table and Simplification — 4M 10M

for logic diagram — 3M

8.b. Explanation of state reduction using equivalence class — 5M 10M

" " " " implication chart — 5M

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ECC235

USN | 2 | B | V | | | | | | | |

III Semester B.E. Examination
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Note: *Answer any TWO full questions from UNIT-I, any TWO full questions from UNIT-II and any ONE full question from UNIT-III.*

UNIT-I

1 a. With the help of neat circuit diagram illustrate the working of a MOS inverter. (6 marks)

b. Solve the following function and represent them in minterm and maxterm canonical form. $f(x,y,z)= x+x'z'(y+z)$ (6 marks)

c Design full adder using minterm generator and maxterm generator. (8 marks)

2 a. There are four doors w,x,y,z for a room. A person cannot enter inside if out of four doors only when

i) Door z is closed

ii) Door y is closed

iii) Door x and y are closed.

iv) Door w,x and y are closed.

v) All are closed.

He is free to decide whether to enter or not, if out of four doors when

i) All are open

ii) Door y, z are closed irrespective of other door conditions, except when all are closed.

iii) Door y, w are closed and x, z are open.

Identify a technique that can be programmed and that is used for more number of variables to generate all possible prime implicates.

Assume: Door closed and person can enter is logic 1.

Door open and person cannot enter is logic 0. (10 marks)

b. Identify the suitable component and using the same design a subtractor, where each number in the subtractor is defined by a binary code of 4 bits. Illustrate with an example. (10 marks)

3 a. Identify a technique that cannot be programmed and that is used for less number of variables to provide minimal sums and minimal products for the following Boolean function.

$f(w,x,y,z)= \Pi M(0,2,6,11,13,15)+dc(1,9,10,14)$ (10 marks)

b. Design a digital system for the following functionality using multiplexers

i) 16:1 mux

ii) 8:1 mux with w,x,y as select lines.

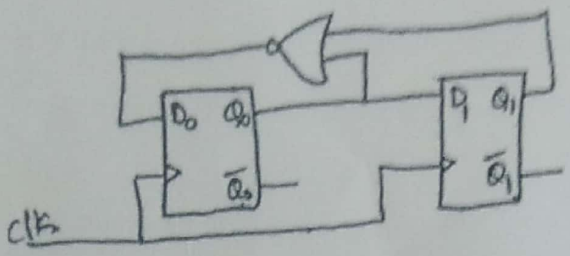
iii) 4:1 mux with w,x as select lines.

$f(w,x,y,z)=\Sigma m(0,1,4,6,7,9,11,14,15)$ (10 marks)

4 a. Realize an SR latch to function as a switch debouncer circuit. (7 marks)

b. Identify the design principle to realize Johnson counter using 4 bit universal shift register. (8 marks)

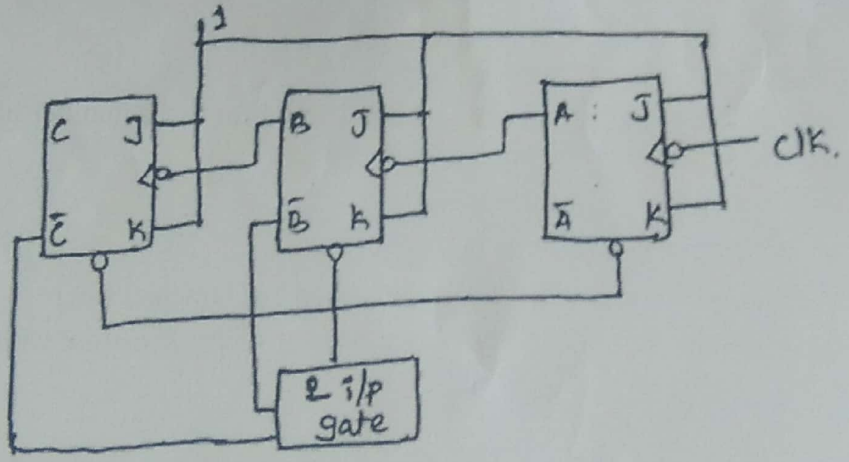
c For the circuit shown in the figure, what will be the sequence of the counter states which Q_1Q_0 follow. (5 marks)



5 a. Mention the limitation of SR flip-flop. How is this limitation overcome using Master-Slave J-K flip-flop? (7 marks)

b. Design a system to provide the status of the number of marbles in a box. It is observed that initially the box was having 3 marbles. Then at regular intervals it was incremented by 1 marble at a time. This repeated till the count increased to 11 marbles. Store this status and demonstrate the count of marbles in the box continuously at all intervals. Use excitation table and data flip-flops. (8 marks)

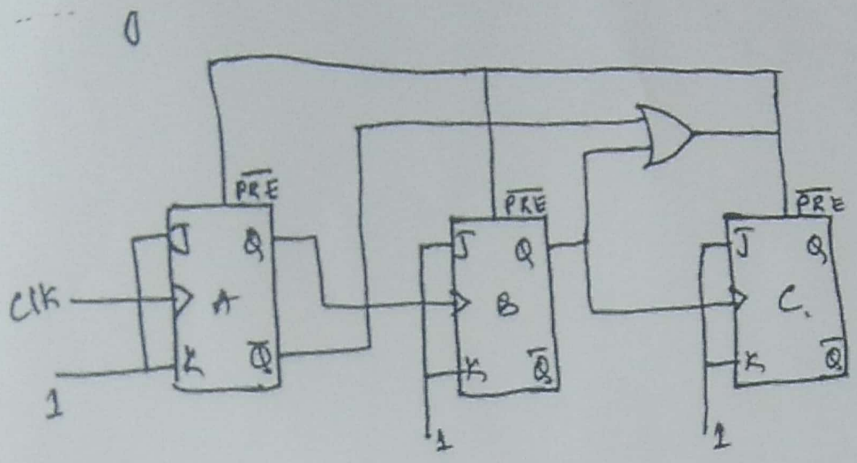
c. In the mod-6 ripple counter shown in the figure, the output of a two input gate is used to clear the JK flip-flop. Identify the gate used. (5 marks)



5 a. Illustrate the functionality of a negative edge triggered D flip-flop using NAND gates. (7 marks)

b. Design an asynchronous mod-5 down counter with initial state being1001. (8 marks)

c Determine the counting sequence for the following counter. (5 marks)



7 a. Compare the Mealy model and Moore model of a clocked synchronous sequential network with a neat block diagram. (10 marks)

b. Illustrate the structure of a clocked synchronous sequential network with a neat diagram. (10 marks)

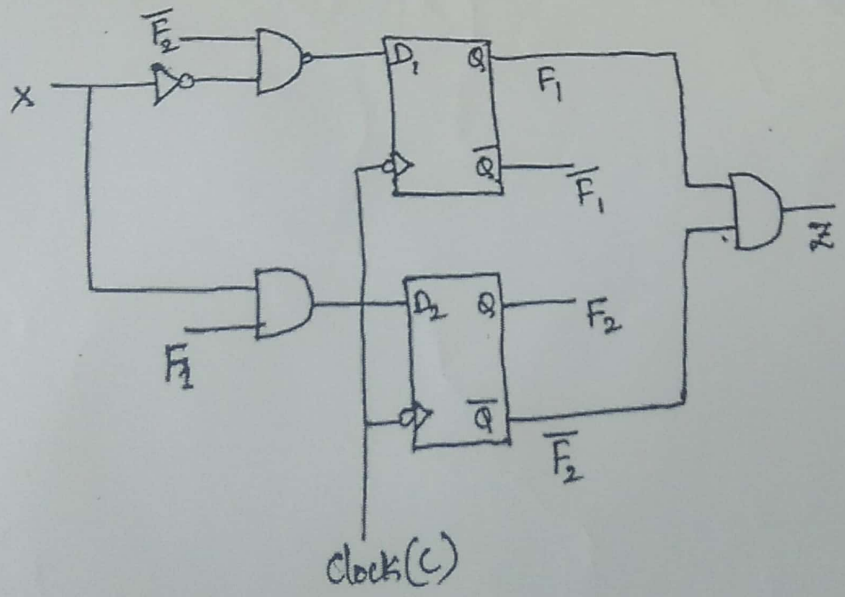
8 a For the logic diagram shown in the figure,

i) Derive the excitation and output equations

ii) Write the next state equations

iii) Construct a transition table and

iv) Draw the state diagram.



(12 marks)

b Explain the following

i) Transition expression

ii) Transition table

iii) Excitation table

iv) State diagram (8 marks)

Set	1	2	3
(Tick √ appropriately)			

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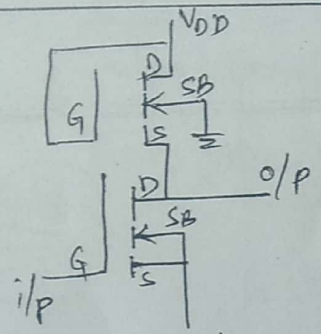
Exam: B.E. / B.Arch. / M. Tech./M.C.A./M.B.A. Academic Program ...B.E.....Sem:...III.....

Course:.....Digital Circuits.....

Course Code:.....ECC235 Duration of Paper:.03 Hrs. Maximum marks:....100.....

Question Number	Solution	Marks Allocated
1 (a)	 2-MOS inverter Diagram → 2 marks, Discussion & operation of 2 MOS inverter → 4 marks	06.
(b)	minterm form, $f(x,y,z) = x + \bar{x}z(y+z)$ $= x + \bar{x}y\bar{z} + \bar{x}z\bar{z}$ $= x(y+\bar{y}) + \bar{x}(y+\bar{y})\bar{z} + \bar{x}y\bar{z}$ $= xy + x\bar{y} + \bar{x}y\bar{z}$ $= xy(z+\bar{z}) + x\bar{y}(z+\bar{z}) + \bar{x}y\bar{z}$ $= xyz + xy\bar{z} + x\bar{y}z + x\bar{y}\bar{z} + \bar{x}y\bar{z}$ 3 Marks +	06.
	Maxterm canonical form $f(x,y,z) = x + \bar{x}z(y+z)$ $= (x+y+z)(x+\bar{y}+\bar{z})(x+y+z)$ 3 Marks	
(c)	Full adder Design using minterm generator & Maxterm generator 8 Marks	08

Question Number	Solution	Marks Allocated

2(a) Tabulation Column. → 3 Marks

Obtaining the function
$f(w,x,y,z) = \Sigma m(4,5,8,9,12,13) + dc(0,3,7,10,11)$ → 1 Mark

S.M reduction → 5 Marks

Prime implicates $\bar{y}$, $w+x$ → 1 Mark

10

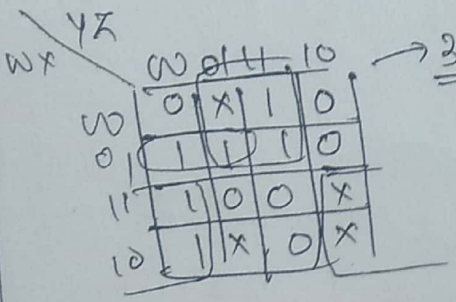
(b) Component → Parallel adder. → 1 Mark

Design of subtractor using parallel adder. → 6 Marks

Illustration of the working with one example subtraction → 3 Marks

10

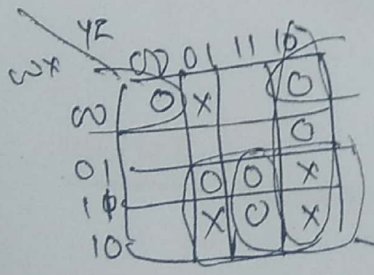
3(a)



→ 3 Marks

$ms_1 = \bar{w}z + w\bar{z} + \bar{w}x\bar{y}$ → 1 Mark

$ms_2 = \bar{w}z + w\bar{z} + x\bar{y}\bar{z}$ → 1 Mark



$mp_1 = (\bar{w}+\bar{z})(\bar{y}+z)(w+x+\bar{y})$ → 1 Mark

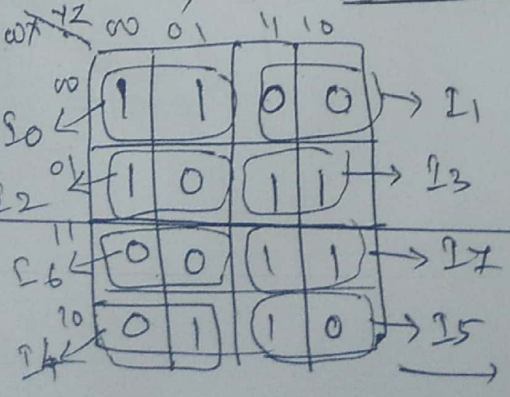
$mp_2 = (\bar{w}+\bar{z})(\bar{y}+z)(w+x+z)$ → 1 Mark

→ 3 Marks.

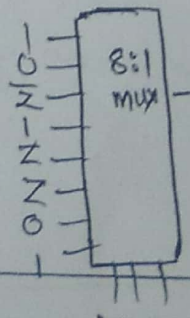
10

3(b) (i) 16:1 mux → 2 Marks

(ii)



→ 2 Marks



→ 2 Marks

Question Number | Solution | Marks Allocated

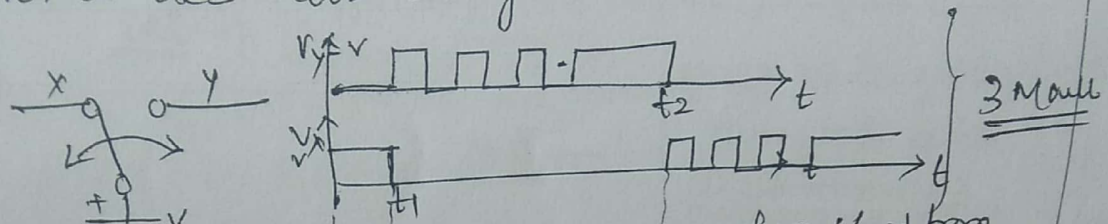
(ii) $f = \bar{y}\,I_0 + (\bar{z}+y)\,I_1 + z\,I_2 + y\,I_3$ → 2 Mark

10

2 Mark

UNIT-II

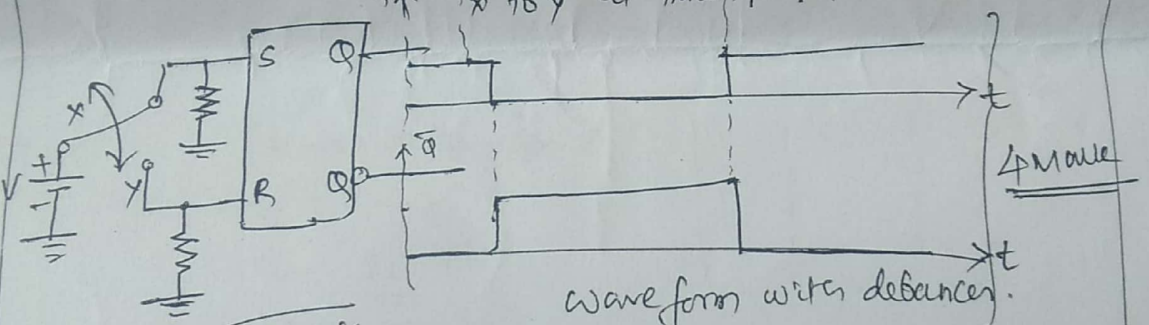
4(a) Switch debaunce using SR latch.



3 Mark

Possible cases at y & x when s/wed from x to y at time t_1 & from y to x at t_2

07

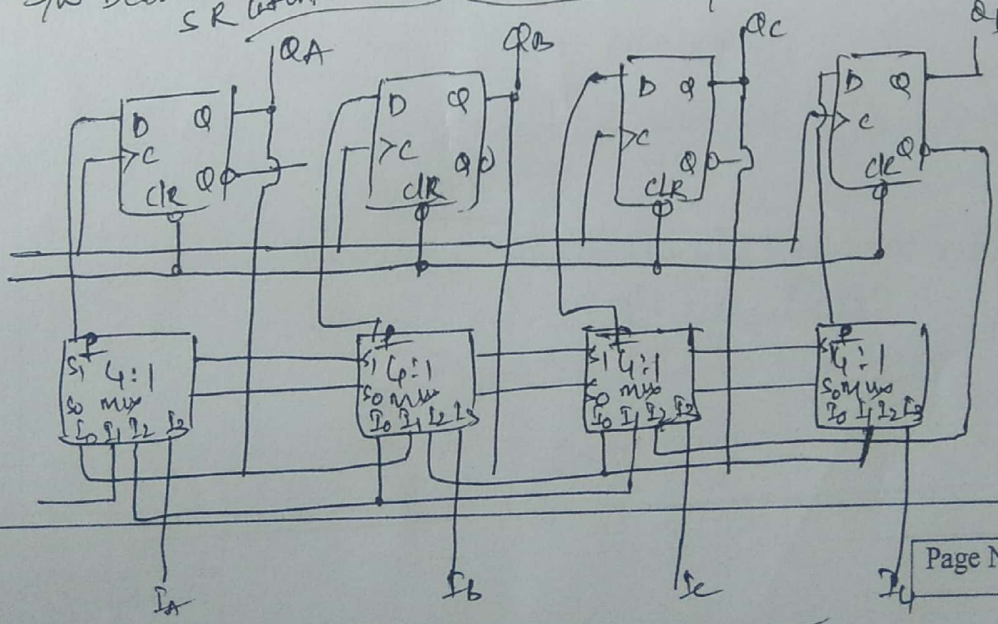


4 Mark

S/w Debaunce using SR latch

waveform with debaunce.

4(b) parallel o/p.



Select lines S_1 S_0	Register operation
0 0	Hold
0 1	Shift right
1 0	Shift left
1 1	Parallel load

08

parallel i/p

Page No. 3/6

Diagram + table → 4 marks . Design principle → 2 Marks

Expln → 2 marks

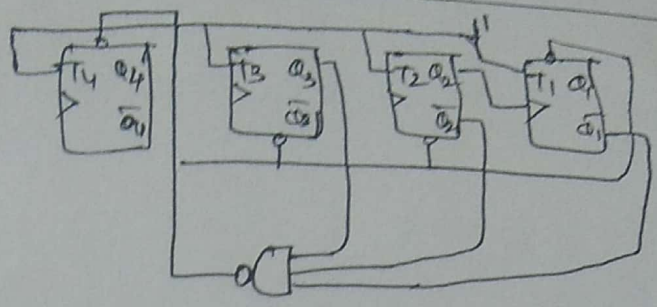
Question Number	Solution	Marks Allocated
4 (c)	Sequence is $00 \rightarrow 01 \rightarrow 10 \rightarrow 00$ → 5 Marks $D_0 = \overline{Q_1 + Q_0}$ $D_1 = Q_0$	05
5 (a)	Limitation → Race around Condition → 1 Mark Master-Slave JK FF Diagram → 2 Marks ↳ Operation showing the remedy for the limitation of SR FF. → 4 Marks	07
(b)	$3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 8 \rightarrow 9 \rightarrow 10 \rightarrow 11$ } → 2M above sequence to be obtained. State diagram, Excitation table + i/p expressions → 4M Implementation circuit → 2M	08
(c)	C B A f 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 0 → 2M for given counter the 2 i/p gate used is OR gate. → 1M Analysis → 2M	05
6 (a)	Negative edge triggered 'D' FF Diagram using NAND gate → 3 Marks + Illustration of functionality with an Example i/p → 4 Marks	07

Question Number	Solution	Marks Allocated

6(b)

Q_1	Q_2	Q_3	Q_4
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0

→ 2 Marks



→ 3 Marks

8M

Design ~~$\bar{Q}_3 \bar{Q}_2 \bar{Q}_1$~~ for P

$P = Q_3 \bar{Q}_2 \bar{Q}_1$ → 3 Marks

(c) Here Clocks of 2nd & 3rd FF are connected to $\bar{Q}$ of previous FF ∴ It is down counter. → 2 Marks

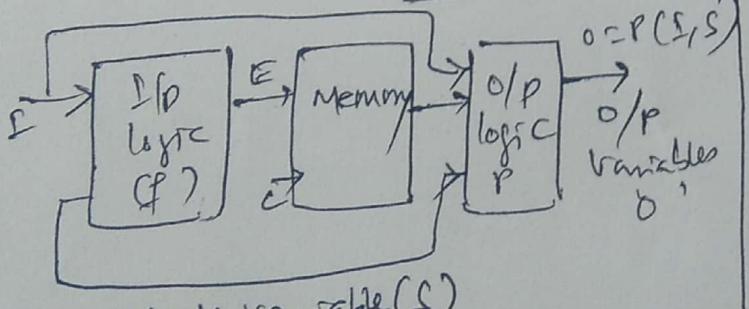
Q_A	Q_B	Q_C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1 → prohibited.
1	1	0
1	1	1

Down counter present.
→ 3 Marks

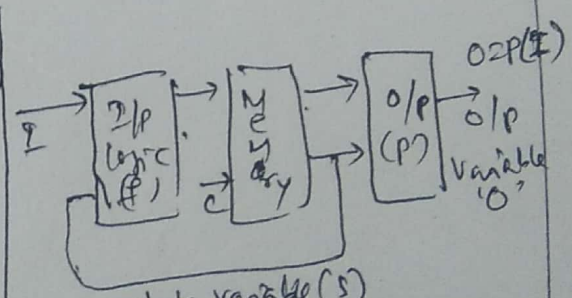
05

UNIT - III

7(a)



2 Marks.



I = I/p variable

3 Marks

Comparison b/w both 4 Marks

10

Question Number	Solution	Mar Alloca

7(b) Clocked synchronous seq n/w structure Diagram → 4 Marks
Illustration / Discussion of working → 6 marks

10

8(a) $D_1 = \overline{F_2}\,\overline{X} = F_2 + X$
$D_2 = F_1 X$
$Z = F_1 \overline{F_2}$
→ 2 Mark

F_1 \ F_2X	00	01	11	10
0	0	1	1	1
1	0	1	1	1

& $D_1 = F_2 + X$

F_1 \ F_2X	00	01	11	10
0	0	0	0	0
1	0	1	1	0

$D_2 = F_1 X$

F_1 \ F_2X	00	01	11	10
0	0	0	0	0
1	1	0	0	0

$Z = F_1 \overline{F_2}$

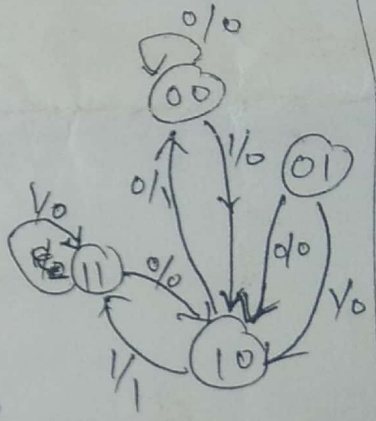
2 Mark

12

$\therefore F_1^+ = D_1$
$F_2^+ = D_2$
→ 1 Mark

Cell no	Present F_1	F_2	X	Next F_1^+	F_2^+	D_1	D_2	o/p Z
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	0
2	0	1	0	1	0	1	0	0
3	0	1	1	1	0	1	0	0
4	1	0	0	0	0	0	0	1
5	1	0	1	1	1	1	1	1
6	1	1	0	1	0	1	0	0
7	1	1	1	1	1	1	1	0

4 Mark



3 Mark

(b) Explanation on
(i) Transition Expression
(ii) " Table
(iii) Excitation "
(iv) State diagram
→ 2 Mark each

8

Dec_2017

17EECC203/17EEEC203

SRN

III Semester B.E. Examination
(Common to EC & EE)
Digital Circuits (17EECC203/17EEEC203)

Duration: 3 hours **Max. Marks: 100**

Note: *i) Answer any TWO full questions from UNIT-I, any TWO full questions from UNIT-II and any ONE full question from UNIT-III.*

UNIT-I

1 a. Explain the working of ECL-OR gate. With the help of circuit diagram. (05marks)

b. Realize the following Boolean expression in minterm and maxterm canonical forms.
$f(x,y,z) = x+x'z'(y+z)$ (05marks)

c Design a circuit using minterm and maxterm generator to realize the following functionality.
$f(w,x,y,z)= \sum m(1,2,6,9,10,14,15)$.
Use only two input external gates. (10marks)

2 a. Three sensors are used to operate two machines. The sensors are labeled as A,B,C. Both machines will not function when none of the sensors are ON. Machine M1 is ON whenever minimum two sensors are ON else no. Machine M2 is ON only when any one sensor is ON. Design a digital system using non programmable logic in SOP and POS formats. (10marks)

b. Realize the following Boolean function with multiplexers.
$f(A,B,C,D)=\sum m(1,3,6,8,10,14,15)$
i) Using 16:1 MUX
ii) Using 8:1 MUX with A,B,C as select lines.
iii) Using 8:1 MUX with A,B as select lines. (10marks)

3 a. Identify a technique that can be programmed and using the same find minimal sums for the following Boolean function.
$f(w,x,y,z)= \prod M(4,6,7,8,12,14)$. (10marks)

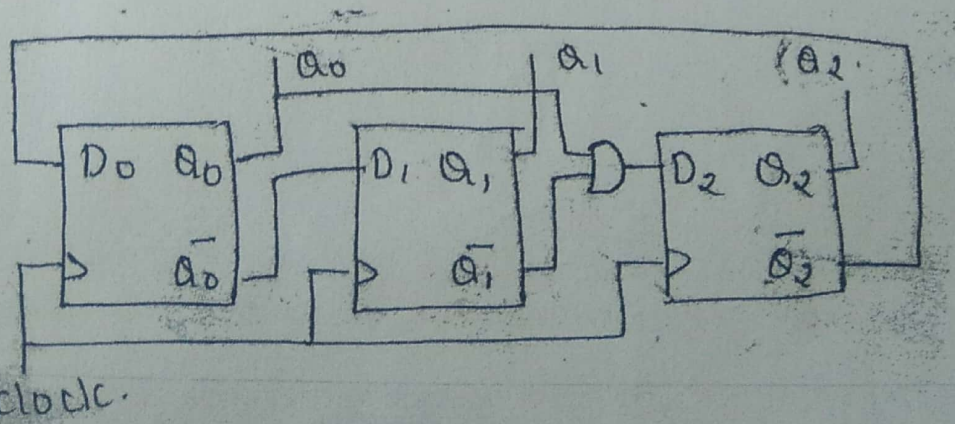
b. Design a digital circuit to compare two digital data by using only one 4 bit magnitude comparator. The length of data is 6 bits each. (10marks)

UNIT-II

4 a. Explain the application of SR latch as switch debouncer. (07marks)

b. Design a universal shift register to realize SISO, PISO by genertaing a bit stream of 1101. (07marks)

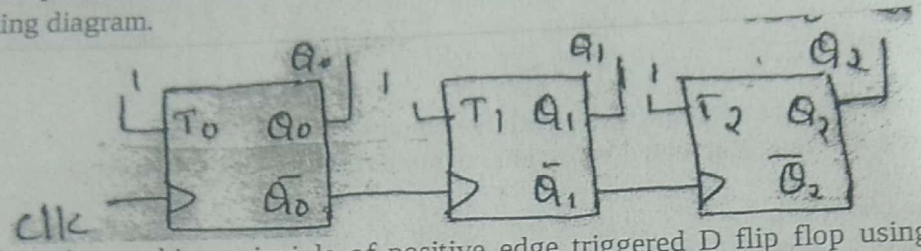
c A sequence generator is shown here. The counter state is initialized to (Q_0, Q_1, Q_2) = (0 1 0). Give the sequence generated at Q_0. (06marks)



5 a. Explain the race around condition. How is it addressed using master slave SR Flip flop. (07marks)

b. Design a 2 bit binary up-down counter using D flip flop. (07marks)

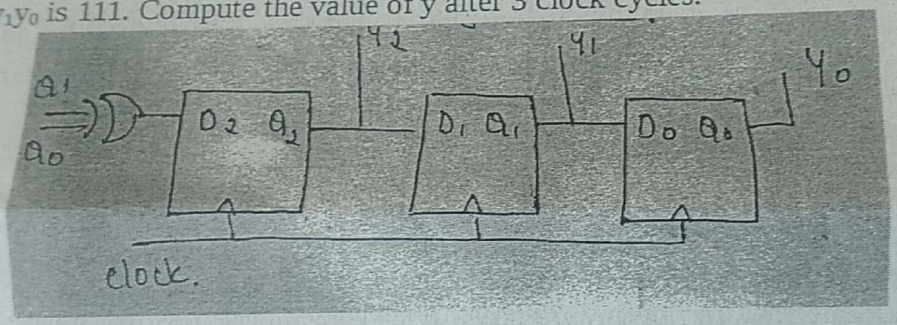
c If the present stae of counter is $Q_2\ Q_1\ Q_0 = 011$ then show the next state using timing diagram. (06marks)



6 a. Explain the working principle of positive edge triggered D flip flop using SR latch. (07marks)

b. Design an asynchronous decade counter to go through a sequence with the initial count of 3 in the increasing order. (07marks)

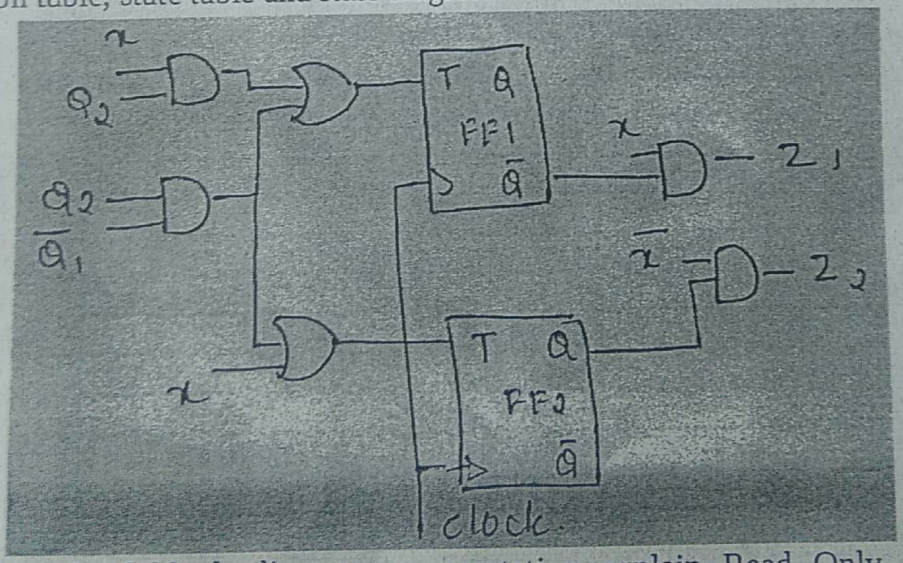
c A three bit pseudo random number generator is shown. Initially the value of $y=y_2y_1y_0$ is 111. Compute the value of y after 3 clock cycles. (06marks)



UNIT-III

7 a. Compare Mealy and Moore models of synchronous sequential networks. (08marks)

b. For the clocked synchronous sequential network construct the excitation table, transition table, state table and state diagram. (12marks)



8 a. With the aid of block diagram representation explain Read Only Memory organization. (10marks)

b. Explain how does a static RAM cell differ from a dynamic RAM cell. (10marks)

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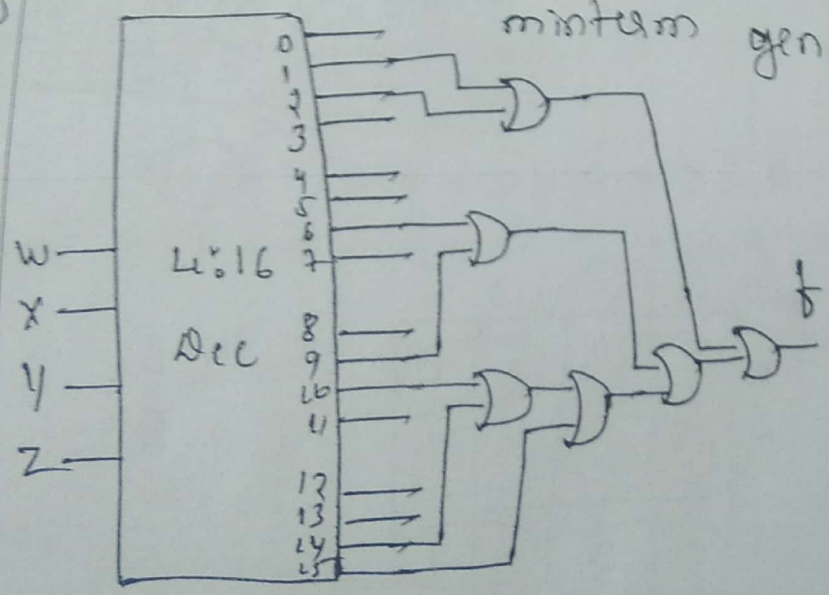
Scheme & Solutions

- A scheme & solution does not mean the splitting of final marks allocated into its component parts (example 2+2+4+2). It has to clearly show the detailed expected answers / response for each component.

Exam: B.E. / B.Arch. / M. Tech./M.C.A./M.B.A./Ph.D Academic Program ECE Sem: III

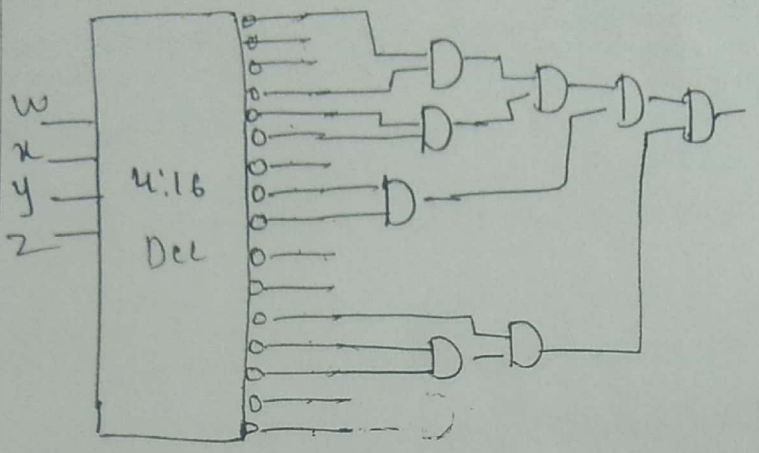
Course: Digital Circuits

Course Code: 17ECE203 Duration of Paper: 3 Hrs. Maximum marks: 100

Question Number	Solution	Marks Allocated
1-(a)	UNIT I Circuit diagram - 2m. Explaination - 3m.	05
(b)	$f(x,y,z) = (x+y+\bar{z})(x+\bar{y}+\bar{z})(x+y+z)$ $= \Pi M(1,3,0)$ - 2½ $= \Sigma m(2,4,5,6,7)$ - 2½.	5m
(c)	minterm generator.  - 5m	10

Question Number	Solution	Marks Allocated

maxterm generator. 5M.



b.

3 (a)

A	B	C	M_1	M_2
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

9M

M_1 =

A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	1

2M

10

$M_1 = BC + AC + AB$ - 1M

$M_1 = (A+C)(A+B)(B+C)$ - 1M

M_2 =

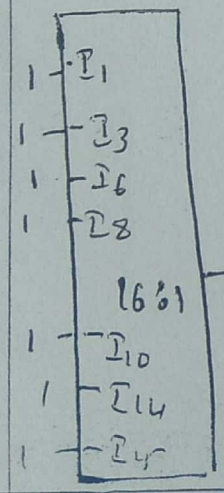
A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	0	0

2M

$M_1 = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$ - 1M

$M_1 = (A+B+C)(\bar{A}+\bar{C})(\bar{A}+\bar{B})(\bar{B}+\bar{C})$ - 1M

(b)



b.

2M

AB \ CD	00	01	11	10
00	0	1	0	0
01	0	0	0	1
11	0	0	1	1
10	1	0	0	1

2M

$I_0 = D$

$I_1 = D$

$I_2 = 0$

$I_3 = \bar{D}$ - 2M

$I_4 = \bar{D}$

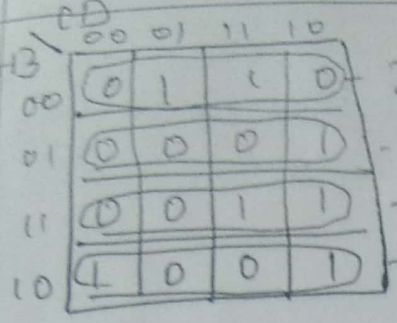
$I_5 = \bar{D}$

$I_6 = 0$

$I_7 = 1$

10

Question Number	Solution	Marks Allocated



- 3m.

ckt diagram -1 m

10

3(a) Using 8m PI's are

$\bar{y}\bar{z}$, wz, $\bar{w}y$, $\bar{w}\bar{z}$, $w\bar{y}$, yz. - 6m.

$MS_2 = \bar{y}\bar{z} + wz + \bar{w}y$ } 4 marks. using

$MS_2 = \bar{w}\bar{z} + w\bar{y} + yz$ Table reduction.

10.

(b)

A_1	A_0	B_1	B_0	L	E	G.
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
1	1	1	1	0	1	0

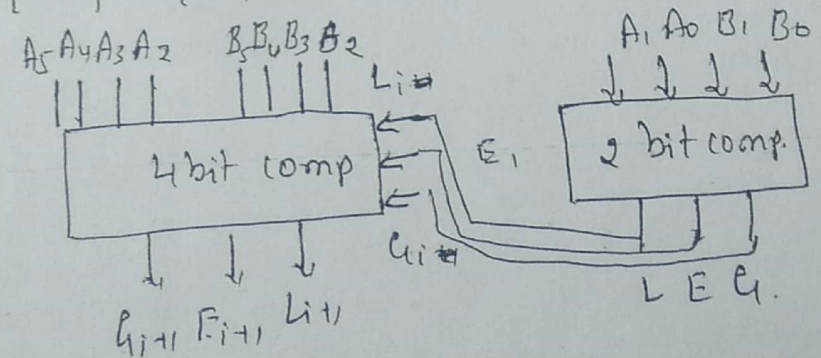
- 2m

$G = A_0 B_1' B_0' + A_1 B_1' + A_1 A_0 B_0'$ -2m

$E = (A_0 \oplus B_0)(A_1 \oplus B_1)$ -2m

$L = \overline{G \oplus E}$. - 1m.

10



- 3m

UNIT - II

4.(a) ckt diagram - 2m.

Timing diagram - 1m.

Explanation - 4m.

07

Question Number	Solution	Marks Allocated
4(b)	USR → ckt diagram - 4M. SISO → 1 M PISO → 1 M Function table - 1M.	7M
(c)	Q_0 Q_1 Q_2 0 1 0 1 1 0 1 0 0 1 0 1 0 0 1 0 1 0 - 2m $D_0 = \bar{Q}_2$ $D_1 = \bar{Q}_0$ $D_2 = Q_0 \bar{Q}_1$ 3m At Q_0 we have 011100..... 1m.	6M
5(a)	Race around condition - 2M. SR - master slave - ckt - 1M. Function table - 1m. Explaination - 3M.	7M
(b)	M Q_1 Q_0 Q_1^+ Q_0^+ D_1 D_0 0 0 0 0 1 0 1 0 0 1 1 0 1 0 0 1 0 1 1 1 1 0 1 1 0 0 0 0 1 0 0 1 1 1 1 1 0 1 0 0 0 0 1 1 0 0 1 0 1 1 1 1 1 0 1 0 0 - up 1 - down - 2m -1m -1m $D_1 = \bar{M}\bar{Q}_1 Q_0 + \bar{M} Q_1 \bar{Q}_0 + M\bar{Q}_1\bar{Q}_0 + M Q_1 Q_0$ $= M \oplus Q_1 \oplus Q_0$ -1m $D_2 = \bar{Q}_0$ - 1 m ckt -1m	07

5(c) $Q_2 Q_1 Q_0$

1 1 1

clk1 0 1 1

clk2 0 0 1

clk3 1 0 0

$D_2 = Q_1 \oplus Q_1$

$D_1 = Q_2$.

$D_0 = Q_1$.

6(a) Ckt diagram - 3m.

Function Table - 1m.

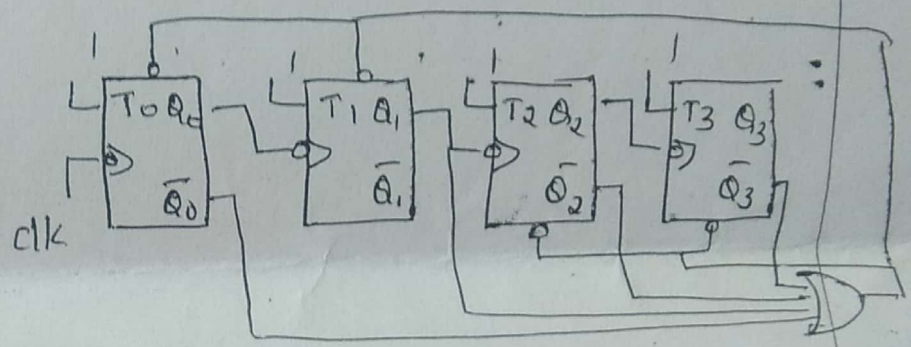
Explaination - 3m.

7m.

(b)

Q_3	Q_2	Q_1	Q_0
0	0	1	1
0	1	0	0
0	1	0	1
1	1	0	0
1	1	0	1

$\bar{Q}_3 + \bar{Q}_2 + Q_1 + \bar{Q}_0 = 0$. - 2m

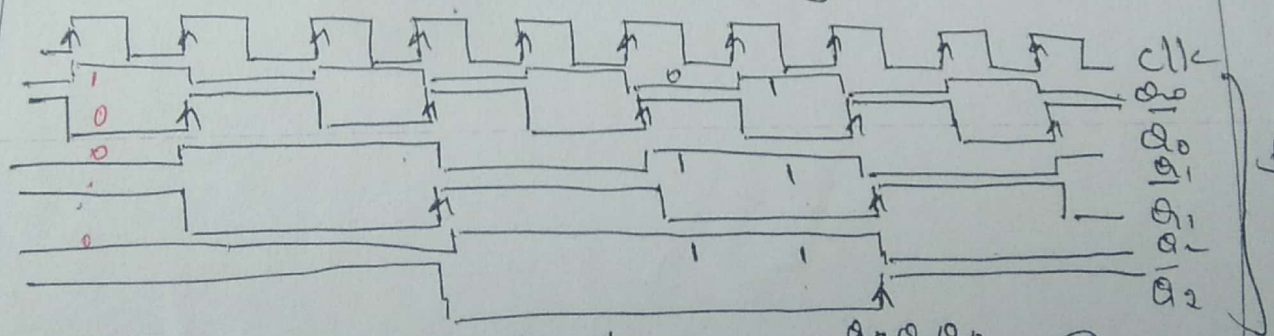


07

- 2m.

- 2m

5.(c)



5m

Illy Q_0, Q_1 & Q_2 to draw. - $Q_2 Q_1 Q_0$ 1 1 1 - (1)

UNIT III

7.(a) 4 comparison points with block diagrams 2M x 4 points.

08m

7.(b) $T_1 = x Q_2 + \bar{Q}_1 Q_2$

$T_2 = x + \bar{Q}_1 Q_2$.

$Z_1 = x Q_1$

$Z_2 = x Q_2$.

- 1M.

Excitation table

$Q_1 Q_2$	$T_1 T_2$		$Z_1 Z_2$	
	0	1	0	1
00	00	01	00	10
01	11	11	01	10
10	00	01	00	00
11	00	11	01	00

- 3M

Transition table.

$Q_1 Q_2$	$Q_1^+ Q_2^+$		$Z_1 Z_2$	
	0	1	0	1
00	00	01	00	10
01	10	10	01	10
10	10	11	00	00
11	11	00	01	00

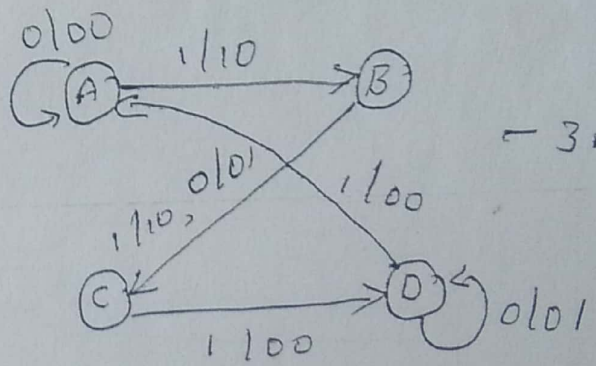
- 3M

State table.

$Q_1 Q_2$	$Q_1^+ Q_2^+$		$Z_1 Z_2$	
	0	1	0	1
A	A	B	00	10
B	C	C	01	10
C	C	D	00	00
D	D	A	01	00

- 2M

State diagram.



- 3M.

8(a) - Block diagram. 4 m. - 10m

Explaination - 6m.

(b) Block diagram - 4m. - 10m

Explaination - 6m.

x

6/6