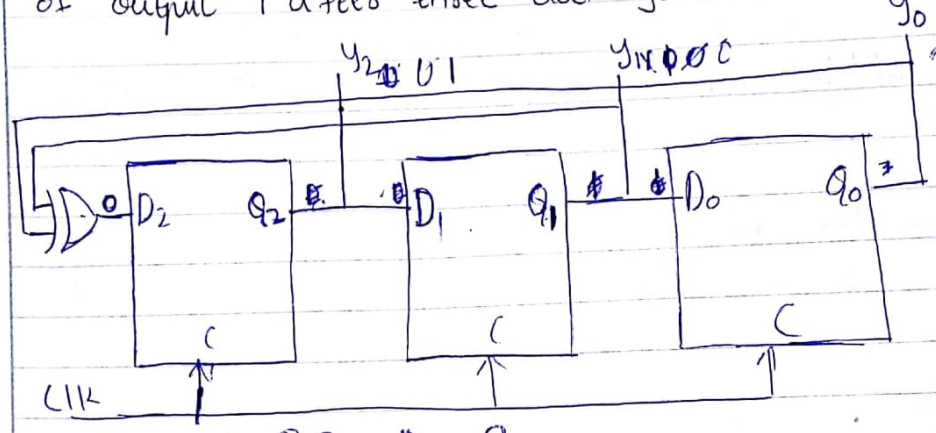
DE GATE QUESTIONS

4. A three bit pseudo random number generator is shown. Initially the value of output $Y = Y_2 Y_1 Y_0$ is set to 111. The value of output Y after three clock cycles is.



$D_2 = Q_0 \oplus Q_1$ $D_0 = Q_1$

$D_1 = Q_2$

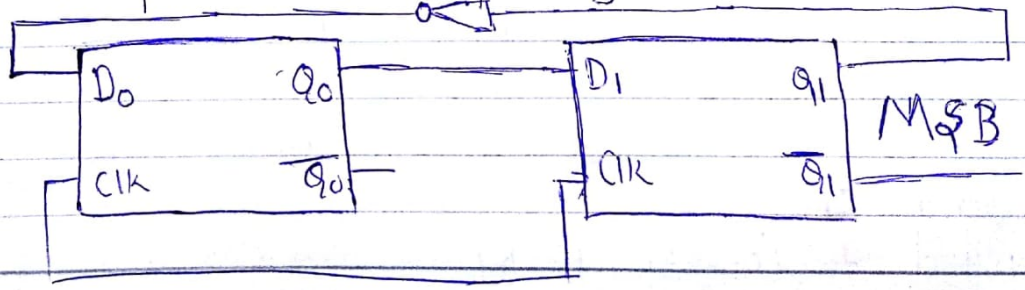
PS			NS			A	B	Y
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	0	0	0
1	1	1	0	1	1 — 1st clock	0	1	1
0	1	1	0	0	1 → 2nd clock	1	0	1
1	0	1	1	0	0 → 3rd clock	1	1	0

Y after 3rd clock is 100

Two D-flip-flops, as shown below are to be connected as a synchronous counter that goes through the following $Q_1 Q_0$ sequence

$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \ldots$

The inputs D_0 & D_1 respectively should be connected as.



	Q_0	Q_1	→	Q_1	Q_0	D_0	D_1	
m_1	0	0		0	0	0	0	initial
m_2	1	0		0	1	1	0	1st clock
m_3	1	1		1	1	1	1	2nd clock
m_4	0	1		1	0	0	1	3rd clock
				0	0	0	0	4th clock.

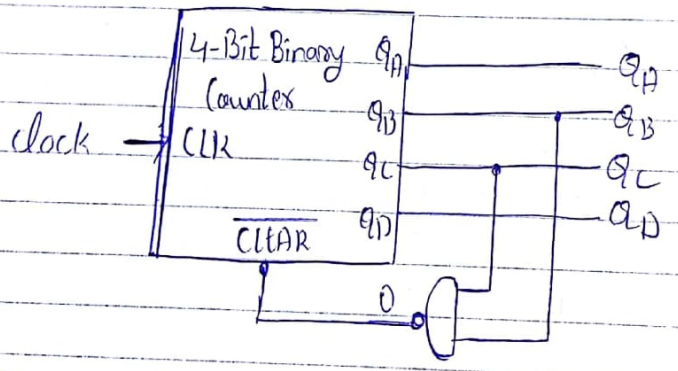
repeats

∴ D_0 should be connected to $\overline{Q_1}$ ⇒ $\overline{Q_0}\,\overline{Q_1} + \overline{Q_1}\,Q_0 = \overline{Q_1}$

D_1 should be connected to Q_0 ⇒ $Q_1 Q_0 + \overline{Q_1} Q_0 = \overline{Q_0}$

Q.M.

A Mod-N counter using a synchronous binary UP counter with asynchronous clear input is shown in fig. The value of N is _____

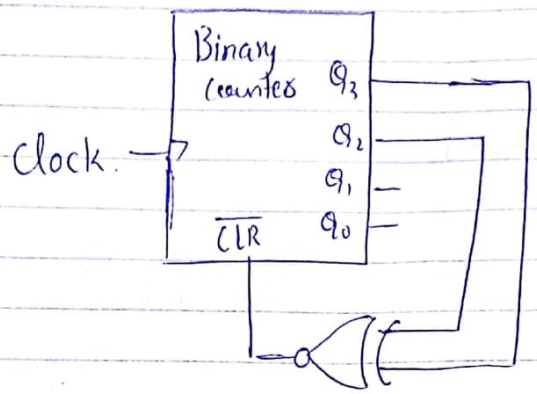


CLK	Q_A	Q_B	Q_C	Q_D	output 0
initial	0	0	0	0	1
1	1	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7th.	0	0	0	0	repeats.

n = 7

Mod-7 Counter (0-6).

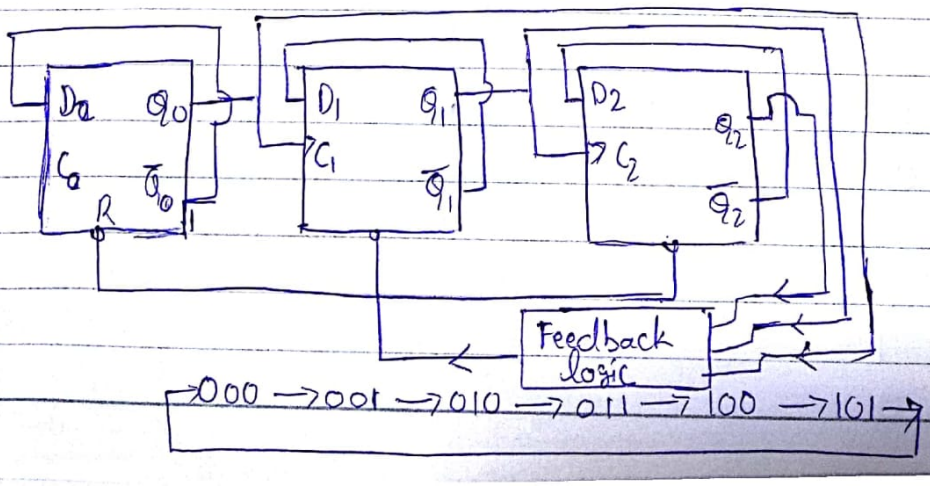
The fig. shows a binary counter with synchronous clear input. With the synchronous clear input. With the decoding logic shown, the counter counts as a _____



Clk	Q_3	Q_2	Q_1	Q_0	$\overline{CLR}$
–	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0

→ MOD 5 Counter (0-4).

A ripple counter using negative edge triggered D-flip-flop is shown below. The flip-flops are cleared at '0' at the R input. The feedback logic is to be designed to obtain the count sequence shown in the same fig. The correct feedback logic is.



a] $F = \overline{Q_2 Q_1 \overline{Q_0}}$ b] $F = Q_2 \overline{Q_1} \overline{Q_0}$

c] $F = \overline{Q_2} \overline{Q_1} Q_0$ d] $F = \overline{Q_2} \overline{Q_1} \overline{Q_0}$

F =

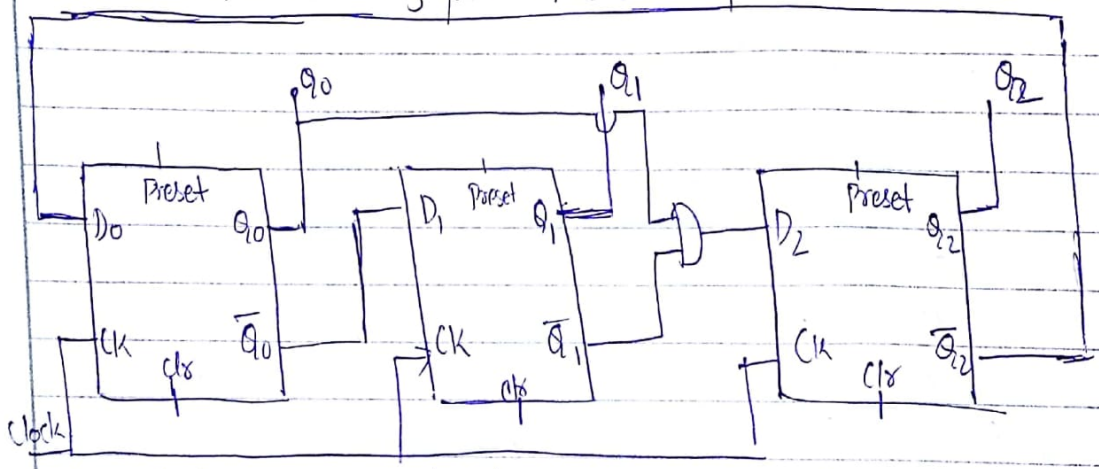
When $Q_2 = 1, Q_1 = 1, Q_0 = 0$

for the that $R = 0$,

=> FF will be reset (000 state)

a] $F = \overline{Q_2 Q_1 \overline{Q_0}}$ (NAND gate)

A sequence generator is shown in fig. The counter status ($Q_0 Q_1 Q_2$) is initialized to 010 using preset / clear inputs.



The clock has a period of 50 ns & transisitons take place at the rising clock edge

a] Give the sequence generators at Q_0 till repeats

b] What is the repetition rate of the generated sequence?

$t_{pr} = 50$ ns.

PS			Next state		
Q_0	Q_1	Q_2	Q_0^+	Q_1^+	Q_2^+
0	1	0	1	1	0
1	1	0	1	0	0
1	0	0	1	0	1
1	0	1	0	0	1
0	0	1	0	1	0
repeats 0	1	0	1	1	0

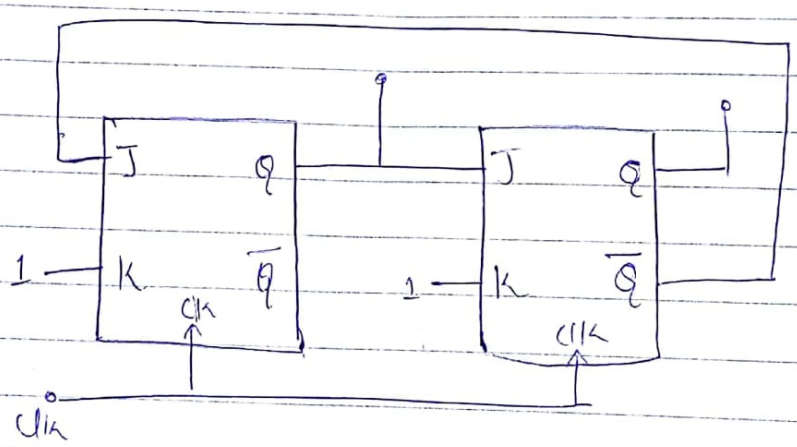
(a) $Q_0 \rightarrow$ 01110, 01110

b] Repeatation takes place every 5 clock (pulse)

5 tpr = 250 ns

repetation rate $= \frac{1}{5\,tpr} = \frac{1}{250\,ns} = 4 \times 10^6$

The fig is shown a mod-k counter, here k is equal to



J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

Q_0	Q_1	Q_0^+	Q_1^+
0	0	1	0
1	0	0	1
0	1	0	0

→ MOD-3 counter (0, 1, 2, 0)

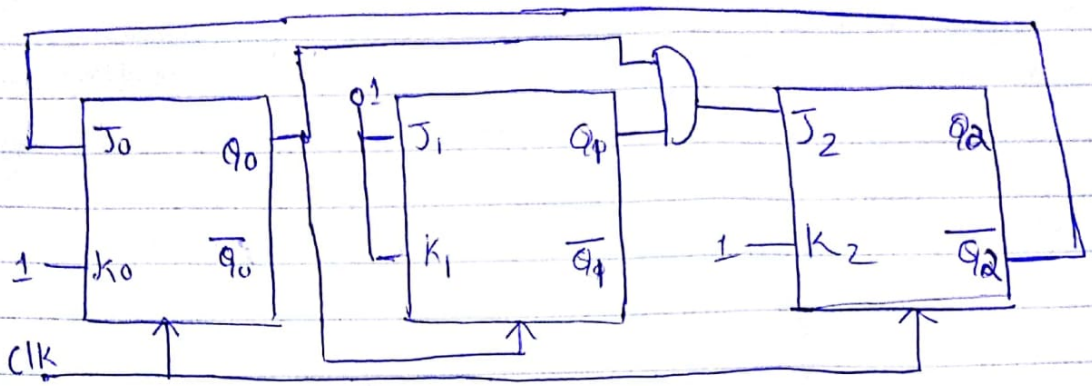
k = 3//

4] The mod 5 counter is shown in the figure counts through states $Q_2Q_1Q_0 = 000, 001, 010, 011$ & 100

a] Will the counter lockout if it happen to be in any one of the unused states?

b] Find the maximum rate at which the counter will operate satisfactorily. Assume the propogation delays of flip-flop & AND

gate to be t_{FF} & t_A respectively.



$J_0 = \overline{Q_2}$ $\quad K_0 = 1$

$J_1 = 1$ $\quad K_1 = 1$

$J_2 = Q_0 Q_1$ $\quad K_2 = 1$

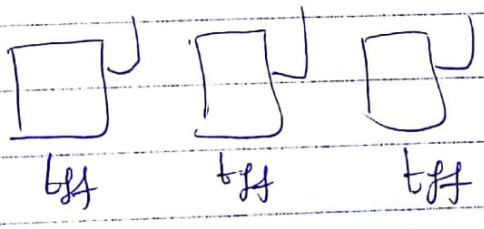
Present state			Inputs (FF)						Next state			
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2^+	Q_1^+	Q_0^+	
1	0	1	0	1	1	1	0	1	0	1	0	(valid state)
1	1	0	0	1	1	1	0	1	0	0	0	(used state)
1	1	1	1	1	1	1	0	1	0	0	0	(used state)

i) ∴ There is no lockout situation.

ii) Minimum time to be maintained blw the two consecutive states

$T_{min} = t_{ff} + t_A$

3 bit asynchronous



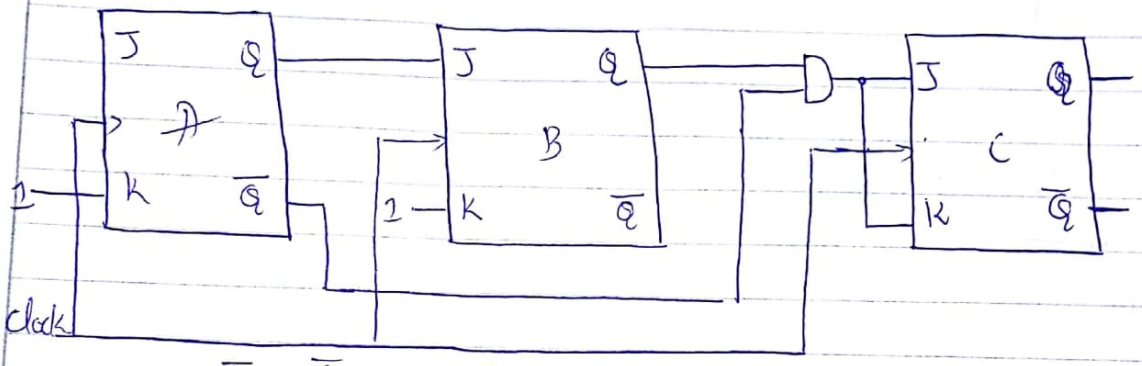
$T_{min} = t_{ff} + t_{ff} + t_A$

(Q_0, Q_2) (Q_0)

$= 2t_{ff} + t_A$.

$$f_{max} = \frac{1}{t_{min}} = \frac{1}{2t_{ff} + t_A}$$

The circuit diagram of an synchronous counter is shown in the given figure. Determine the sequence of states of the counter assuming that the initial state is 000. Give your answer in a tabular form showing the present state Q_A, Q_B, Q_C, J-K inputs ($J_A, K_A, J_B, K_B, J_C, K_C$) & the next state Q_{A+1} Q_{B+1} Q_{C+1}. From the table, determine the modulus of the counter.



$J_A = \overline{Q}_B$ $\quad K_A = 1$

$J_B = Q_A$ $\quad K_B = 1$

$J_C = Q_B \overline{Q}_A$ $\quad K_C = Q_B \overline{Q}_A$

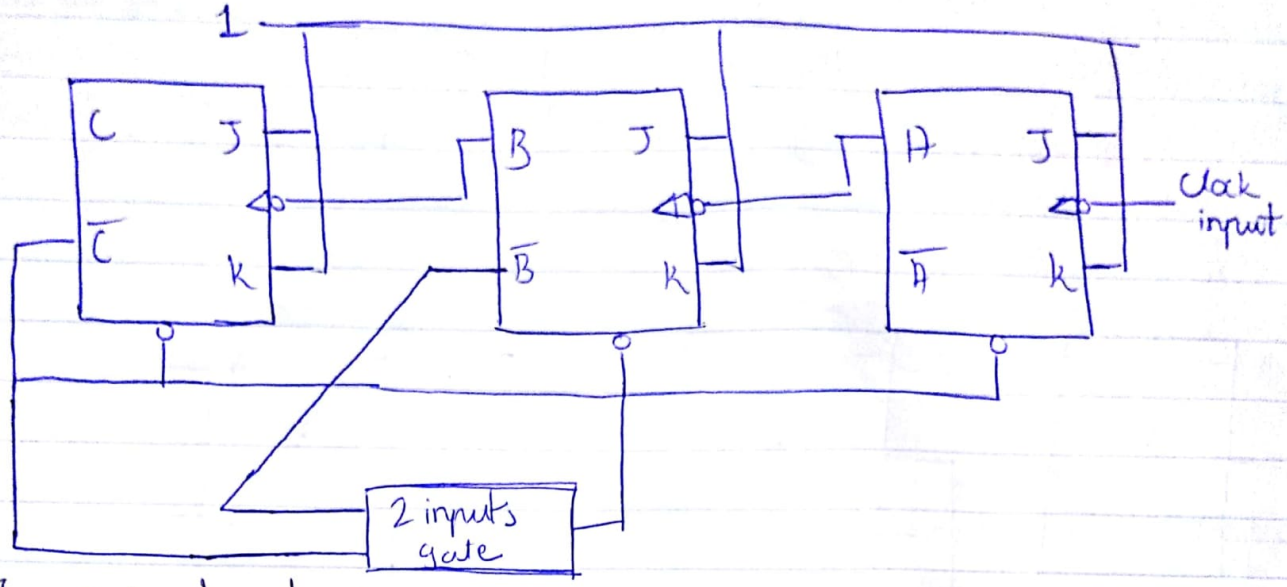
Present state			Inputs (flip flop)						Next state		
Q_A	Q_B	Q_C	J_A	K_A	J_B	K_B	J_C	K_C	Q_A^+	Q_B^+	Q_C^+
0	0	0	1	1	0	1	0	0	1	0	0
1	0	0	1	1	1	1	0	0	0	1	0
0	1	0	0	1	0	1	1	1	0	0	1
0	0	1	1	1	0	1	0	0	1	0	1
1	0	1	1	1	1	1	0	0	0	1	1
0	1	1	0	1	0	1	1	1	0	0	0

0 → 4 → 2 → 1 → 5 → 3

6 states.

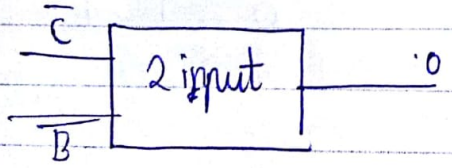
∴ it is Mod 6 counter

In the modulo-6 ripple counter shown in the given fig. the output of the 2 input gate is used to clear the JK flip-flops.



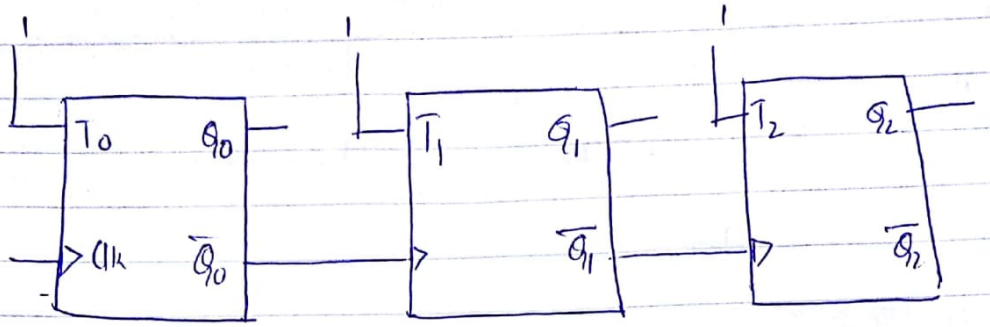
The 2 input gate is
a] NAND gate
b] NOR gate
c] OR Gate
d] AND gate

(B A = 0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1 } used states
1 1 0 } unused states



Ans- OR Gate

The given figure shows a ripple counter using edge triggered flip flops. If the present state of the counter is $Q_2Q_1Q_0 = 011$, then it's next state $Q_2Q_1Q_0$ will be

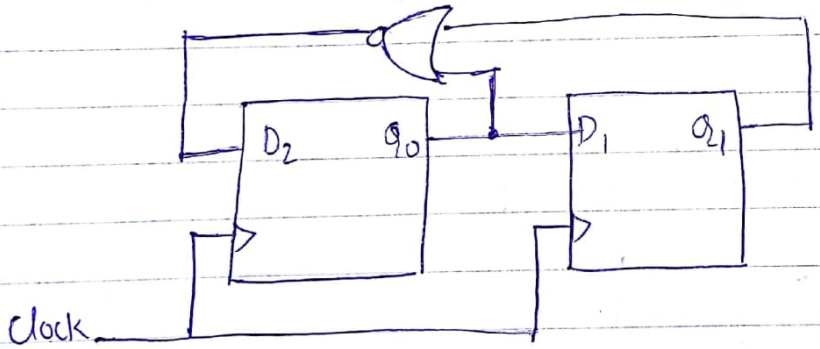


Present state			Next state		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+
0	1	1	1	0	0

when $T = 1$

then complement of the present state output.

For the circuit shown, the counter state (Q_1Q_0), follows the sequence



a] 00, 01, 10, 11, 00 ....

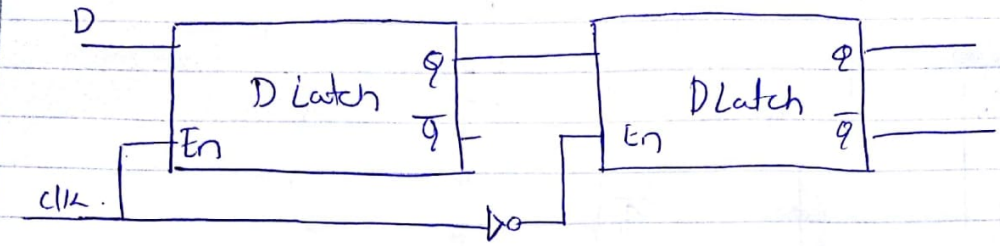
b] 00, 01, 10, 00, 01 ....

c] 00, 01, 11, 00, 01 ....

d] 00, 10, 11, 00, 10 ....

D_0	D_1	Q_0	Q_1	Q_1 Q_0
0	0	0	0	0 0
1	0	1	0	0 1
0	1	0	1	1 0
0	0	0	0	0 0
1	0	1	0	then repeats.

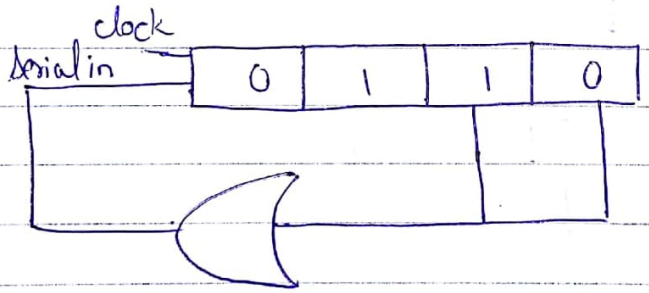
The circuit shown in the fig. is a



a] Toggle flip flop
b] JK flip flop
c] S & R Latch
d] Master - Slave D flip flop.

Ans :- d] Master - Slave D flip flop.

The initial contents of the 4 bit serial in serial out, right shift, register shown in fig. are 0110. After three clock pulses are applied the contents of the shift register will be.



a] 0000
b] 0101
c] 1010
d] 1111

Q_3	Q_2	Q_1	Q_0		$Q_3^{\uparrow}$	$Q_2^{\uparrow}$	$Q_1^{\uparrow}$	$Q_0^{\uparrow}$
0	1	1	0	1st	1	0	1	1
					0	1	0	1
					1	0	1	0

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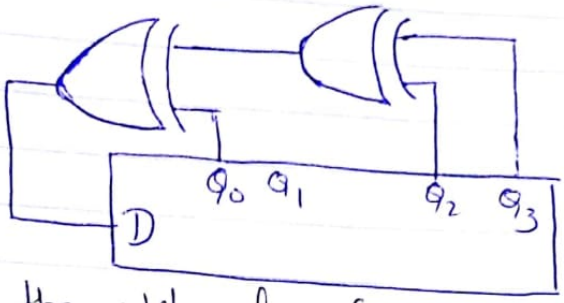
A 4 bit shift register, which shifts 1 bit to the right a every clock pulse, is initialized to values 1000 for ($Q_0 Q_1 Q_2 Q_3$). The D input is derived from Q_0, Q_2 & Q_3 through two XOR gates as shown in fig.



a] Write the 4bit values ($Q_0 Q_1 Q_2 Q_3$) after each clock pulse till the pattern (1000) reappears on ($Q_0 Q_1 Q_2 Q_3$).

b] To what values should the shift register be initialized so that the pattern (1001) occurs after the first clock pulse?

Ans:-

D ($Q_0 \oplus Q_2 \oplus Q_3$)	clock	Q_0 Q_1 Q_2 Q_3
—	—	1 0 0 0 (initial)
1	1	1 1 0 0
1	2	1 1 1 0
0	3	0 1 1 1
0	4	0 0 1 1
0	5	0 0 0 1
0	6	1 0 0 0 Sequence repeats.

after 1st clock pulse

Q_0 Q_1 Q_2 Q_3

D Q_0 Q_1 Q_2 $\Rightarrow$ 1001 $\Rightarrow$

$Q_0 = 0$ $Q_1 = 0$ $Q_2 = 1$

$D = 1 = Q_0 \oplus Q_2 \oplus Q_3$

$\Rightarrow D = 1 = 0 \oplus 1 \oplus Q_3$

$Q_3 = 0$

$\therefore$ Answer - 0010