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Introduction.

Digital design flow.

- Full custom flow
- Semi custom flow
- Memory flow
- ASIC

Full custom flow: Specification, logic design and implementation.

- Schematic ~~layout~~ design
  - pre simulation - to check functionality
- Layout → DRC → LVS. (layout vs schematic)
- parasitic extraction → post simulation (to find rise & fall time)

$$t_r = 2.2\, T_p$$

$$T_p = RC.$$

- After post & pre layout simulation, the design is fabricated.

Semi custom flow: Pre defined library files called standard cells are used to design a schematic / layout.

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This method is used to save market time. These are intellectual properties.

- ASIC - Application specific integrated circuit

These are used because general purpose design may have cons such as more power, memory & cost consumption and less efficiency. These again usually use semi-custom flow.

- Memory flow: Used only when specifications are provided by the user.

Flow is defined as: An effective methodology of capturing & verifying.

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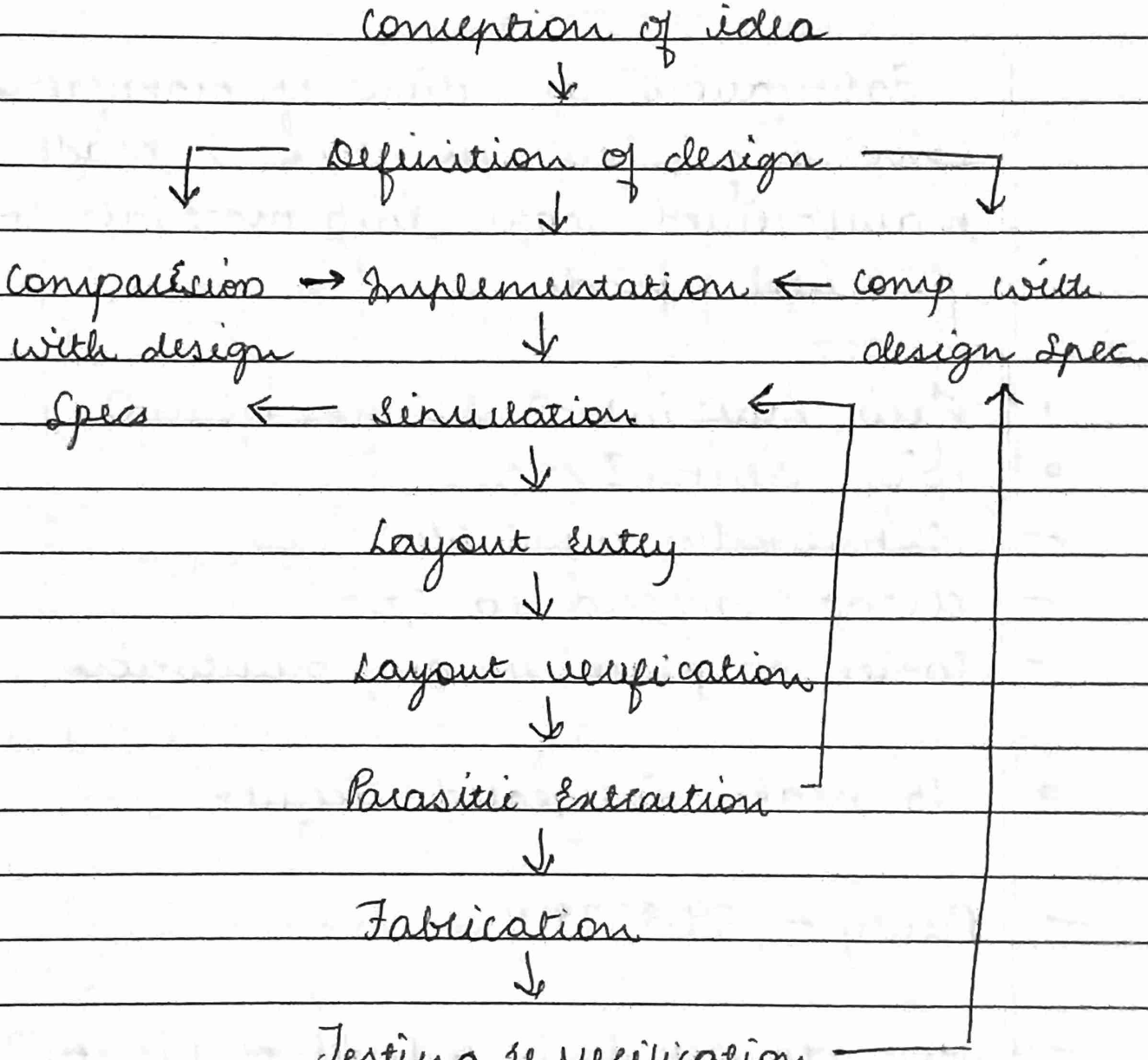
Custom IC design flow



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Introduction To CMOS fabrication

Fabrication is action of manufacturing something, when an item is made or manufactured from raw materials to finished goods.

- Raw material → silicon (Sand)
- Why silicon?
  - Abundantly available
  - Cheap compared to Ge
  - Easier to place in any orientation
- To make integrated circuits.
- Purity - 99.99999%
- How to get such a level of purity?
  → CZ method. (Fig 1.) [Sand to Silicon]
- Wonder why? Silicon wafer is circular shape? Because cutting ends would be waste of silicon since they are circular from start.

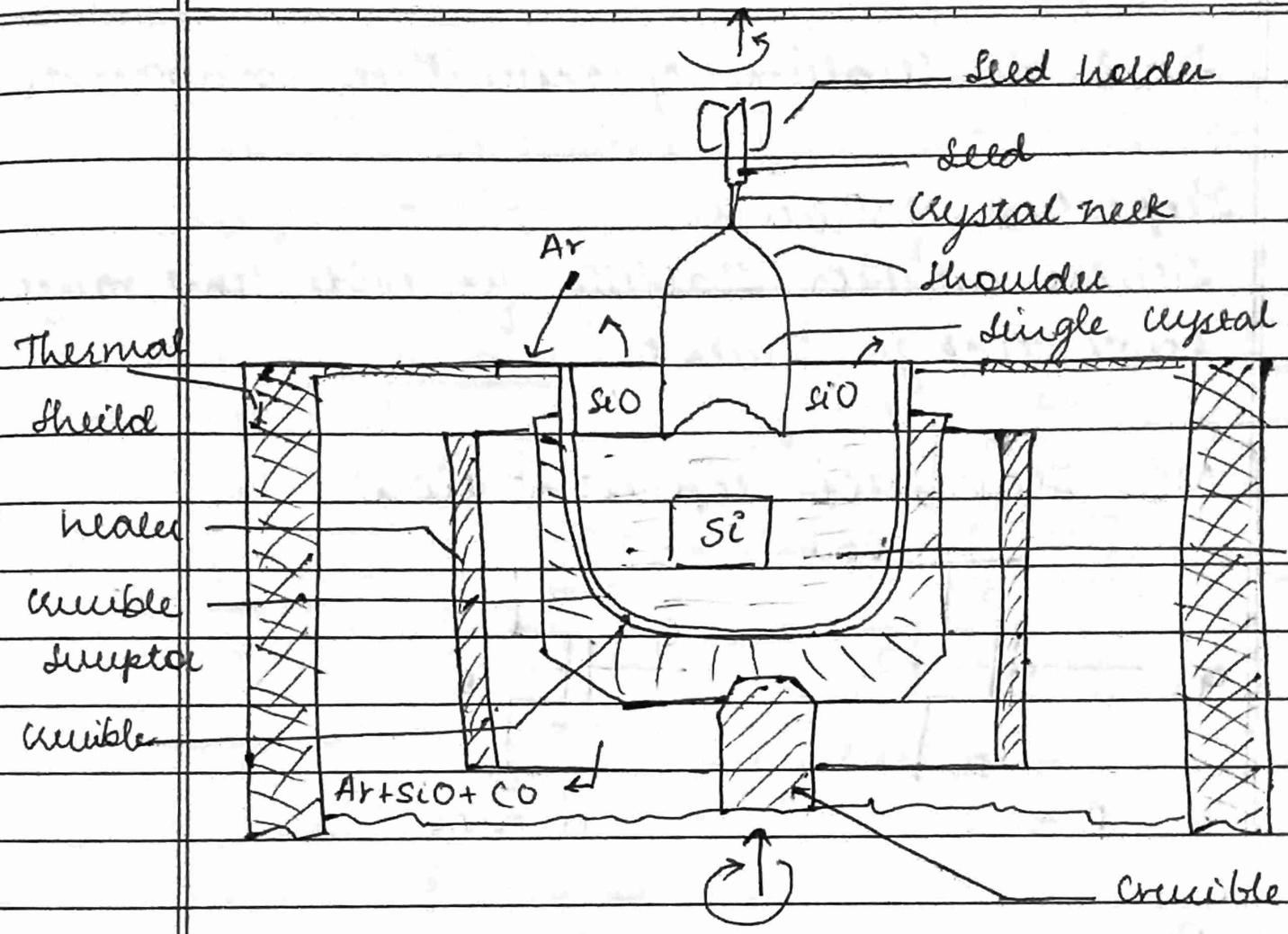

Fig. 1. Beginning of crystal growth.

Why Semiconductor?

- Conductivity between conductor & insulator
- conductivity can be adjusted with doping
  - n type - n^+ n n^-
  - p type - p^+ p p^-
- p^+ / n^+ heavily doped. - p^- / n^- lightly doped.
- p | n moderately doped.

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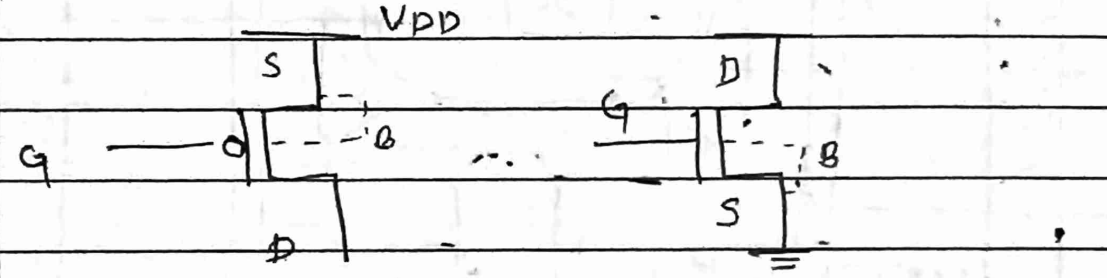
- lead to creation of miniature components.

Properties of Silicon:

- Silicon exhibits stability for wide temp range
- lower leakage current

MOS Transistor representation.



- Positive photo resist — Formation of source & drain
- Negative photo resist - formation of gate.

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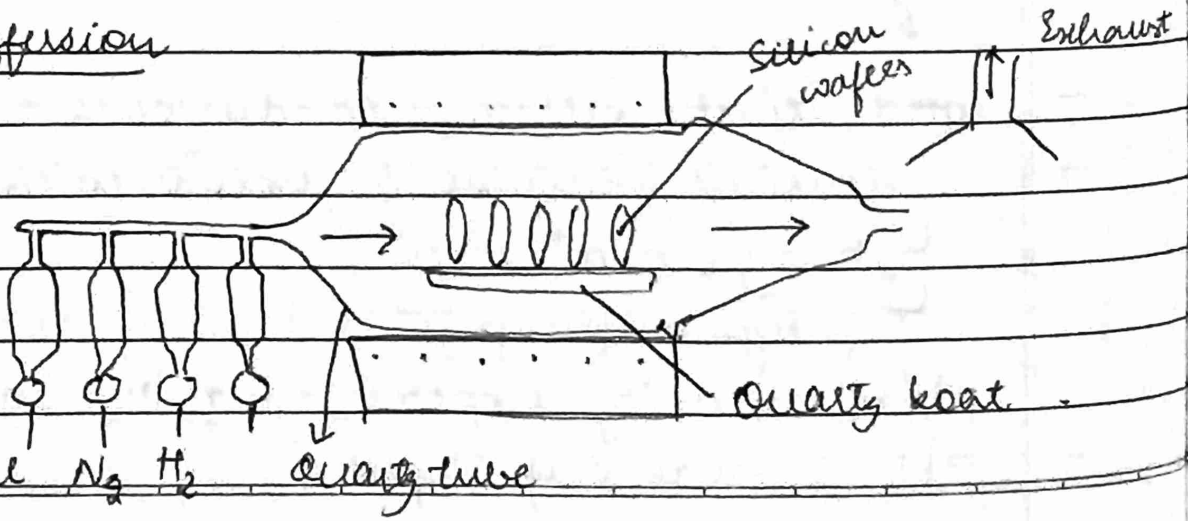
Diffusion



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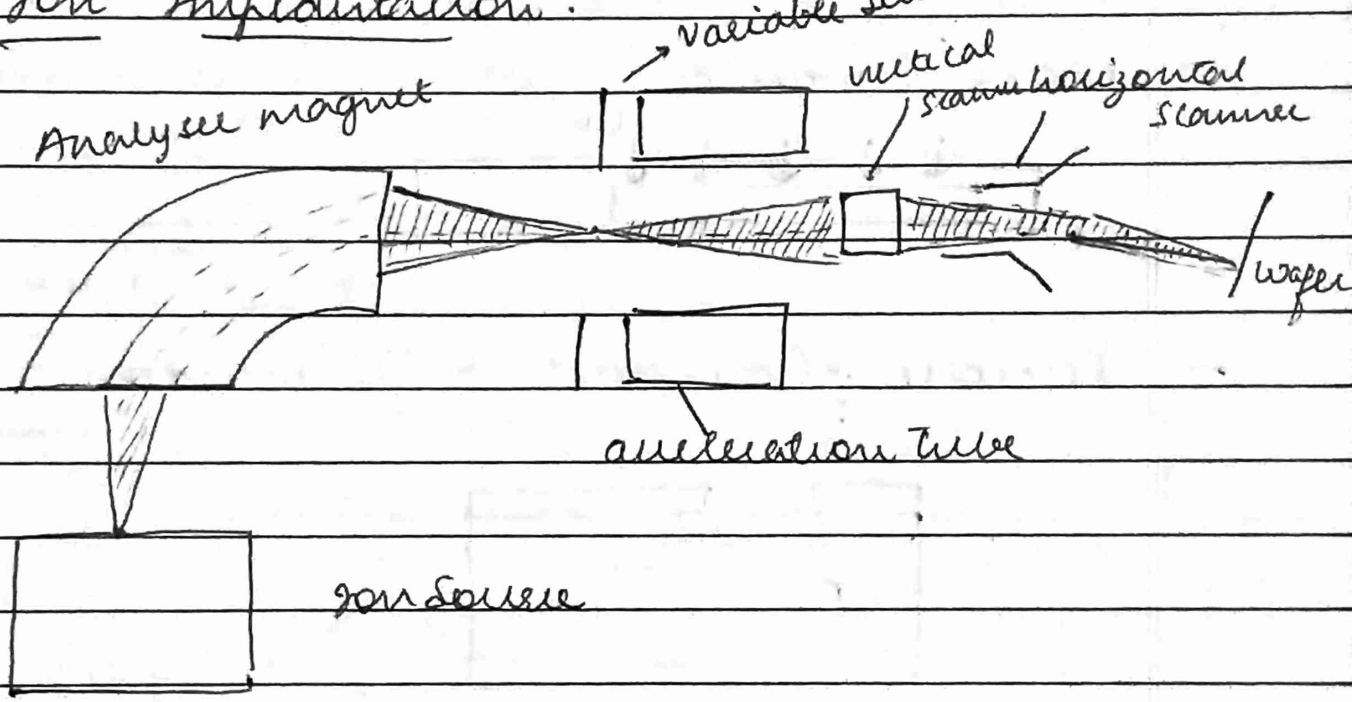
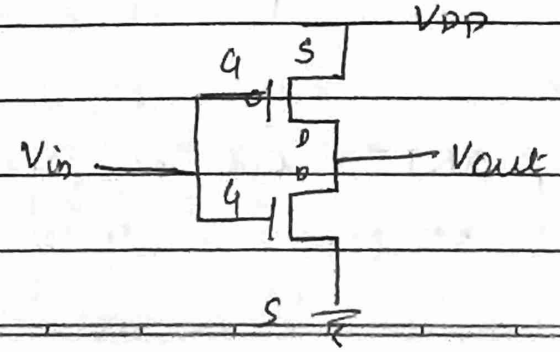
In diffusion, the concentration of doping may not be as desired. Hence, we move to ion implantation.

Ion Implantation.



In this doping method, we get a desired doping concentration on wafer.

Fabrication process of CMOS inverter.



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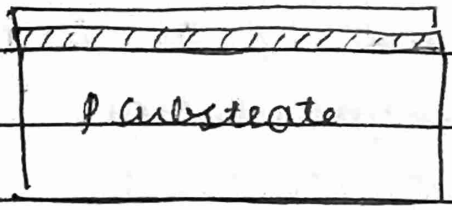
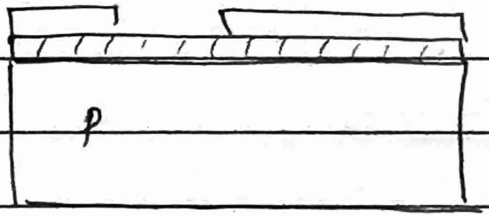
Step 1:

- P substrate
- Thick SiO_2
- Neg Positive photoresist

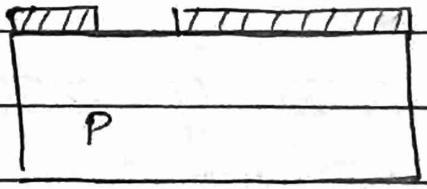


- Mask & window

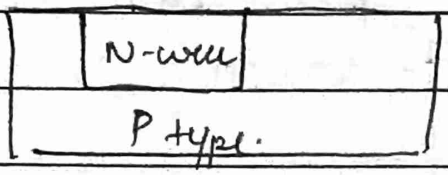
- Remove photoresist over window



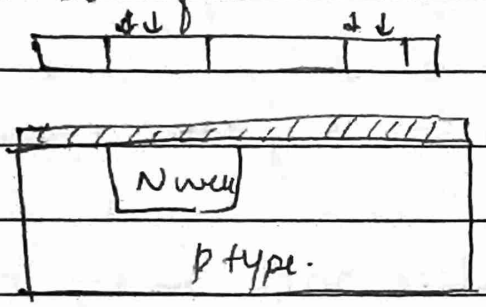
Step 2: Remove soluble SiO_2 layer completely



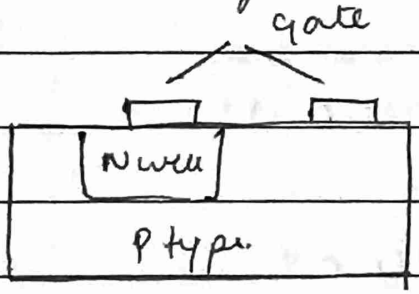
Step 3: Ion implantation for forming N-well & remove SiO_2 layer



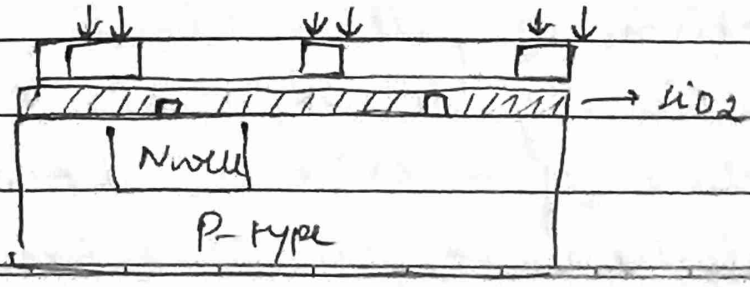
- Form a thin SiO_2 layer & apply negative photo resist to form the gate.

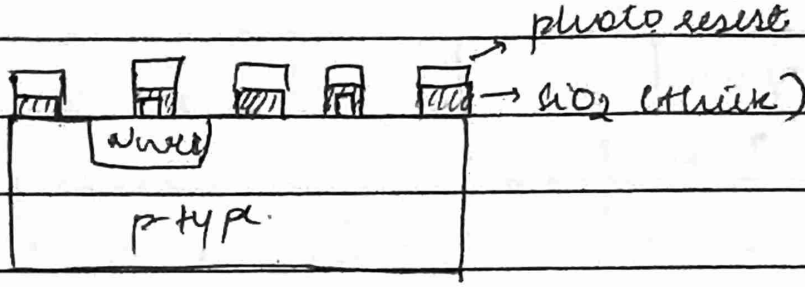


- From UV rays, solidify the gates for P & N-mos



- Form a field oxide (thick oxide) for source & drain. Take another mask. firstly for p-mos & then n-mos.





- Similarly for n-mos, same process is taken
- Remove the photo resist from drain & source
- Apply poly layer over gate using mask
- Apply pselect (p+ mask over entire layer of the wafer.
- Similarly apply Nselect/n+.

Brief of N-well method.

- P substrate, oxide (SiO_2), Photoresist (+ve)
- Mask (n well or p well)
- Ion implantation for n-well/p-well
- Formation of gate (thin SiO_2 layer)
- Formation of source, drain & bulk (pMOS)
- Formation of S, D & B of n-mos
- Metalization to form the connection

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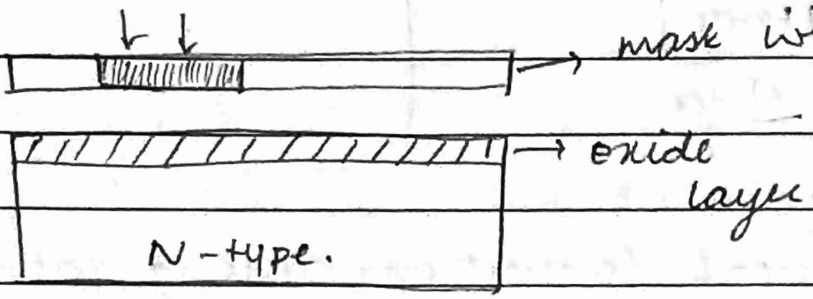
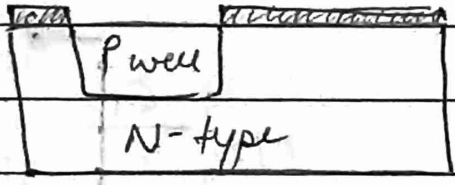
P-well method

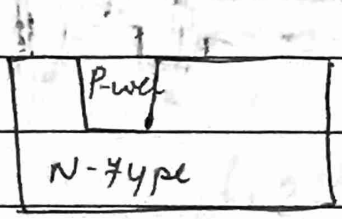
1.



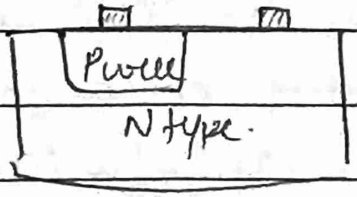
2. The masked region for a p-well region.



3] Ion implantation of p type give a p well. & the excess SiO_2 is removed.

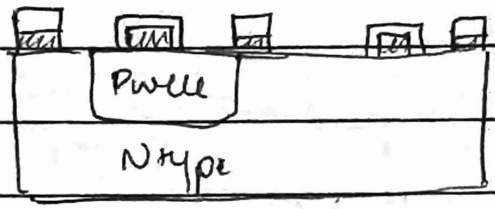


4] Form a thin SiO_2 layer for gate formation

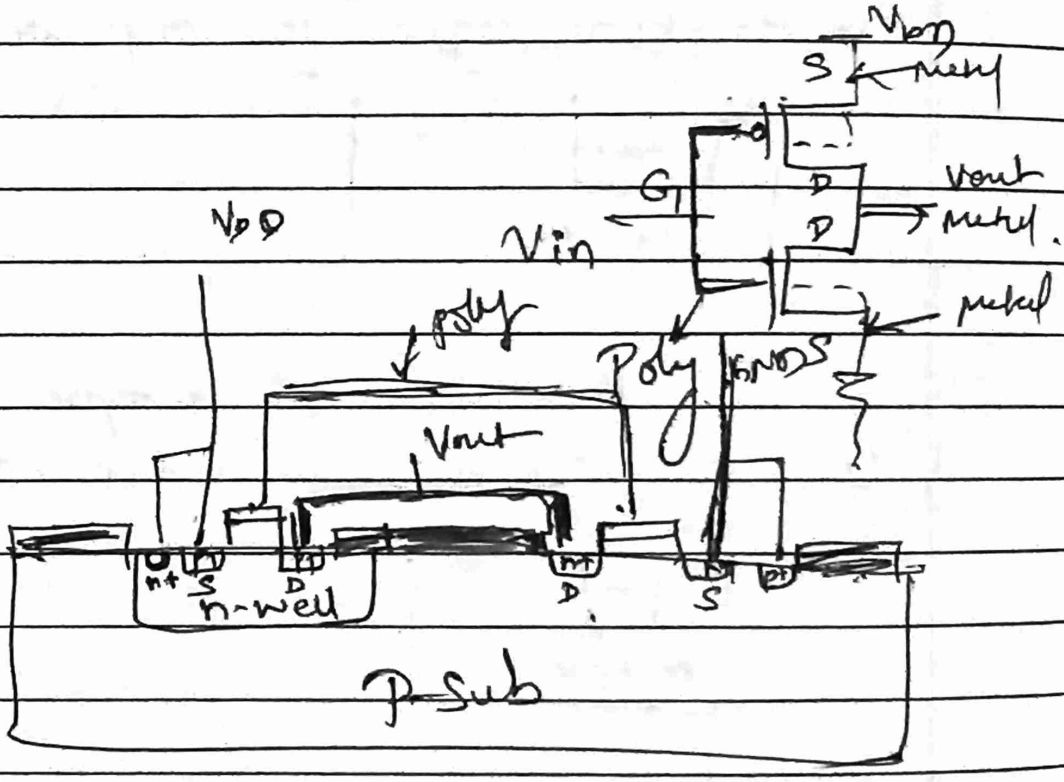


(negative photoresist)

5) Form a thick SiO_2 layer (positive photoresist) for source & drain.



- Form metal connections among gates & of p & n and drain (metalization)



The gates are connected using poly to metal connection. The drains are connected by putting a mask & adding metal for connection. Similarly sources & bulk are shorted with VDD or ground.

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Activity 1.

1. What is VLSI.

→ Very large scale integration of circuits.

2. What is design capture?
3. Why is an IC design flow termed as custom
4. What is the meaning of full custom flow and why is the flow cannot be used in larger design?
5. What is the meaning of 3D extraction? What is the technology node at which the VLSI industries are presently working?
6. List the top ten global VLSI companies & the EDA tools used by them.?
7. What are parasitic & how does it influence the performance characteristics of design
8. What is meant by RTL design? State its importance.
9. What is standard cell library? Where do we use?
10. Can we do a simulation before implementation

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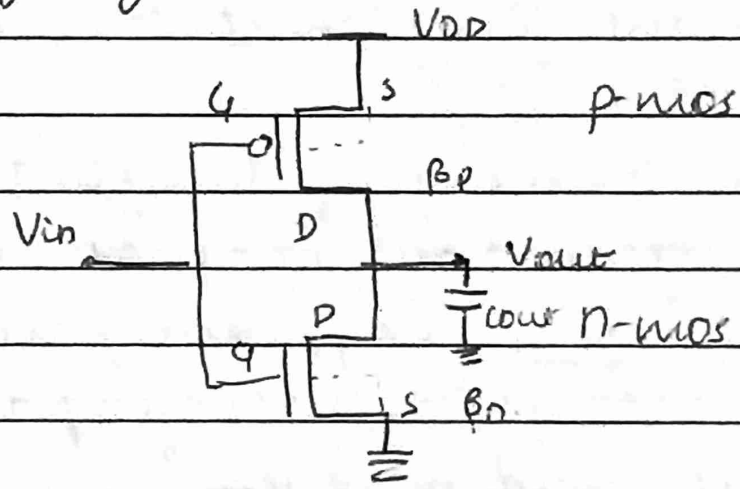
2. 2.

CMOS Inverter (Static)

1) DC Characteristics

$y = \bar{y}$ y — $\bar{y}$

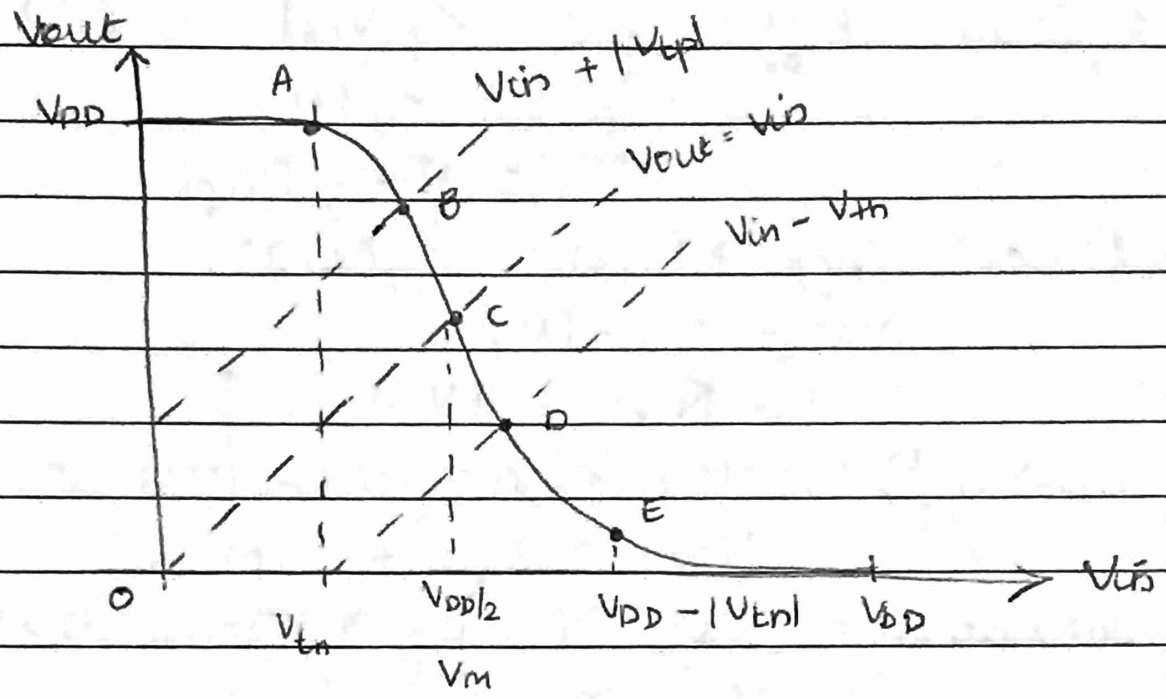


Transient : Varying wrt time

Aspect ratio $\beta_p = k_p' \left(\frac{W}{l}\right)_p$; $k_p' = \mu_p C_{ox}$

$\beta_n = k_n' \left(\frac{W}{l}\right)_n$; $k_n' = \mu_n C_{ox}$

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_0 \epsilon_{si}}{t_{ox}}$



n-mos: $V_{gs_n} = V_g - V_s$

$= V_{in} - 0$

$V_{gsn} = V_{in}$

$V_{dsn} = V_d - V_s$

$V_{dsn} = V_d = V_{out}$

Regions: cut off: $V_{in} < V_{tn}$ (A)

Triode: $V_{in} > V_{tn}$ (D, E)

& $V_{DS} < V_{in} - V_{tn} \Rightarrow V_{out} < V_{in} - V_{tn}$

Saturation: $V_{gsn} > V_{tn}$, (B, C)

$V_{dsn} \geq V_{in} - V_{tn}$

p mos: $V_{sgp} = V_s - V_g$

$= V_{DD} - V_{in}$.

$V_{sdp} = V_s - V_d = V_{DD} - V_{out}$.

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Region: Cutoff : $V_{sgp} < |V_{tp}|$ (E)

$V_{DD} - V_{in} < |V_{tp}|$

$V_{in} > V_{DD} - |V_{tp}|$

Linear : $V_{sgp} > |V_{tp}|$ (A, B)

$V_{DD} - V_{in} > |V_{tp}|$

$V_{in} < V_{DD} - |V_{tp}|$

(V_{sdp}) $V_{DD} - V_{out} < V_{DD} - V_{in} - |V_{tp}|$

$V_{out} > V_{DD} + |V_{tp}|$

Saturation : $V_{sg_p} > |V_{tp}| \Rightarrow V_{DD} - |V_{tp}| > V_{in}$.

$V_{sdp} \geq V_{sgp} - |V_{tp}|$

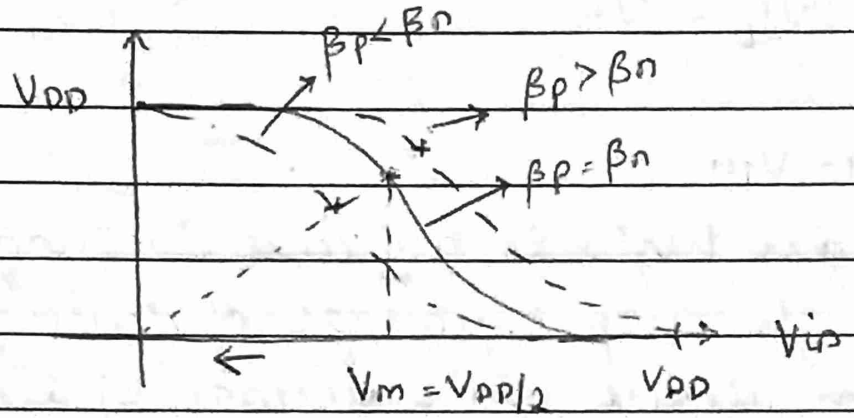
$V_{DD} - V_{out} \geq V_{DD} - V_{in} - |V_{tp}|$.

$V_{out} \leq V_{in} + |V_{tp}|$ (C, D)

Region	nmos	pmos	Region	n	p
Cutoff	$V_{in} \leq V_t$	$V_{in} \geq V_{DD} - V_t$	A	Cutoff	triode
triode	$V_{in} > V_t$	$V_{in} < V_{DD} - V_t$	B	Sat	triode
Sat	$V_{out} < V_{in} - V_t$	$V_{out} > V_{in} + V_t$	C	Sat	Sat
Sat	$V_{in} > V_t$	$V_{in} < V_{DD} - V_t$	D	triode	Sat
	$V_{out} \geq V_{in} - V_t$	$V_{out} \leq V_{in} + V_t$	E	triode	cutoff

Also, $\beta_p \propto (W/L)_p$ & $(W/L)_n \propto \beta_n$

As width increases, Vout halts more time at V_{DD} ($\beta_p > \beta_n$)



The above graph shows β-ratio effect.

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Noise Margin

The minimum/maximum amount of noise a device can withstand without affecting the output is called noise margin.

- It is a parameter closely related to the input/output characteristic.
- This parameter allows us to determine the allowable noise voltage on input of a gate, so that, the output will not be affected.
- N_{ML} – Noise margin low is defined as difference in magnitude between maximum low output voltage of the driving gate & maximum input low voltage recognized by the driven gate.

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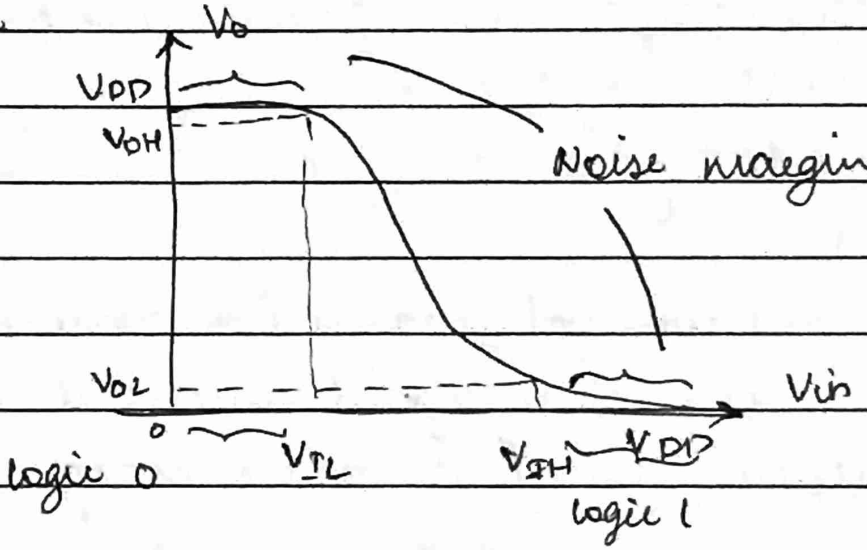
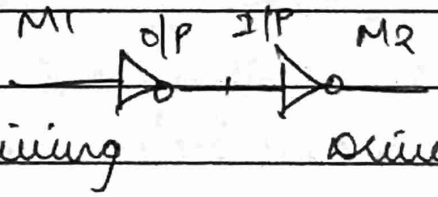
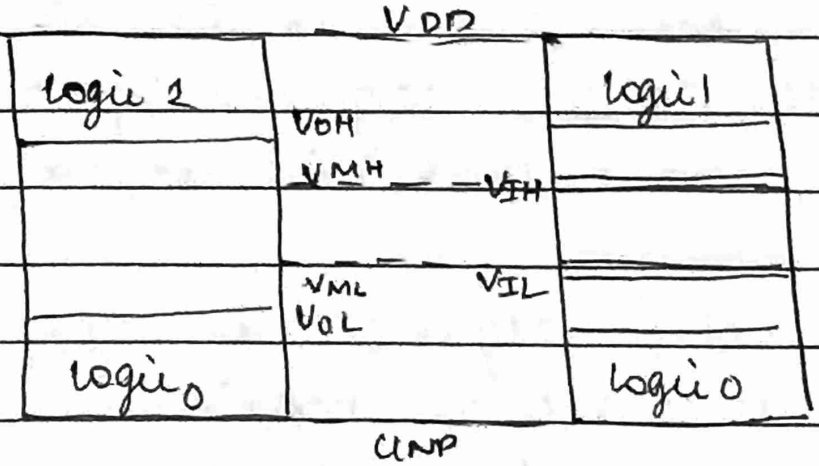
$NM_L = V_{IL} - V_{OL}$

– $NM_H = V_{OH} - V_{IH}$

Noise margin high is difference in magnitude between high output voltage of driving gate & minimum input high voltage of receiving gate.







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i) $V_{TH} \uparrow$

$\uparrow N_{ML} = \uparrow V_{IL} - V_{OL}$

ii) $V_{IH} \uparrow$

$\downarrow N_{MH} = V_{OH} - V_{IH} \uparrow$

- Noise margin depends on β ratio of MOS

Mid point Voltage.

Both MOS should lie in saturation region

$\therefore I_{Dn} = \frac{\beta_n}{2}(V_m - V_{tn})^2$

$I_{Dp} = \frac{\beta_p}{2}(V_{DD} - V_m - |V_{tp}|)^2$

$\frac{\beta_n}{2}(V_m - V_{tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_m - |V_{tp}|)^2$

$\beta_n (V_m^2 + V_{tn}^2 - 2V_m V_{tn}) = \beta_p ((V_{DD} - V_m)^2 + (|V_{tp}|)^2$

$\Rightarrow \sqrt{\beta_n}(V_m - V_{tn}) = \sqrt{\beta_p}(V_{DD} - V_m - |V_{tp}|)$

$V_m \sqrt{\beta_n} - \sqrt{\beta_n} V_{tn} = \sqrt{\beta_p} V_{DD} - \sqrt{\beta_p} V_m - \sqrt{\beta_p} |V_{tp}|$

$V_m (\sqrt{\beta_n} + \sqrt{\beta_p}) = \sqrt{\beta_p}(V_{DD} - |V_{tp}|) + \sqrt{\beta_n} V_{tn}$

$$V_m = \frac{\sqrt{\beta_p}(V_{DD} - |V_{tp}|) + \sqrt{\beta_n} V_{tn}}{\sqrt{\beta_n} + \sqrt{\beta_p}}$$

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$$V_M = \frac{V_{DD} - |V_{tp}| + \sqrt{\beta_n/\beta_p}\, V_{tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

For $|V_{tp}| = V_{tn}$ & $\beta_p = \beta_n$

$$\boxed{V_M = \frac{V_{DD}}{2}}$$

- Consider a CMOS process with parameters
$k_n' = 140\,\mu A/V^2$, $k_p' = 60\,\mu V^{-2}A$, $V_{tn} = 0.7V$
$V_{tp} = -0.7V$, $V_{DD} = 3V$

i) $\beta_n = \beta_p$, find V_m

ii) Using given parameter find β_p & β_n & find V_m

i) $\beta_p = \beta_n$

$$V_M = V_{DD} - \frac{|V_{tp}|}{2} + V_{tn} = 3 - \frac{0.7}{2} + 0.7$$

$$V_M = 1.5V$$

ii) for $\beta_n = k_n' (W/L)_n$ & $\beta_p = k_p' (W/L)_p$

$k_p' (W/L)_p = k_n' (W/L)_n$ [Relative]

$$(W/L)_p = \frac{k_n'}{k_p'} (W/L)_n$$

$$(W/L)_p = 2.33\,(W/n)_n$$

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If $(W/L)_p = (W/L)_n$, $\beta_n/\beta_p = ?$

$\beta_n/\beta_p = 2.33$.

$$V_M = \frac{3 - |0.7| + \sqrt{2.33} \times 0.7}{1 + \sqrt{2.33}}$$

$$= 1.33V$$

- A CMOS inverter is built in a process $K_n' = 100\mu A V^{-2}$, $K_p = 42 A V^{-2}\mu$, $V_{tn} = 0.7V$, $V_{tp} = -0.8$, $V_{DD} = 3.3V$. Find V_M for $(W/L)_n = 10$, $(W/L)_p = 14$

→ $\beta_n = 100 \times 10$

$\beta_p = 42 \times 14$.

$\beta_n/\beta_p = 1.7$

$$V_M = \frac{3.3 - |0.8| + \sqrt{1.7} \times 0.7}{1 + \sqrt{1.7}} = 1.483\ V$$

- Find the ratio $\beta_n/\beta_p = ?$, for $V_M = 1.3V$ with $V_{DD} = 3V$, $V_{tp} = -0.82V$ $V_{tn} = 0.6V$. what would be the relative device size if $K_n' = 110\mu A/V^2$ & mobility values are related $\mu_n = 2.2\mu_p$.

→ $\mu_n = 2.2\mu_p$

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{ox} (W/L)_n}{\mu_p C_{ox} (W/L)_p} \qquad \frac{\beta_n}{\beta_p} = 1.58$$

$$1.58 = 2.2 \frac{(W/L)_n}{(W/L)_p}$$

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$(W/L)_p = 1.4 \ (W/L)_n$

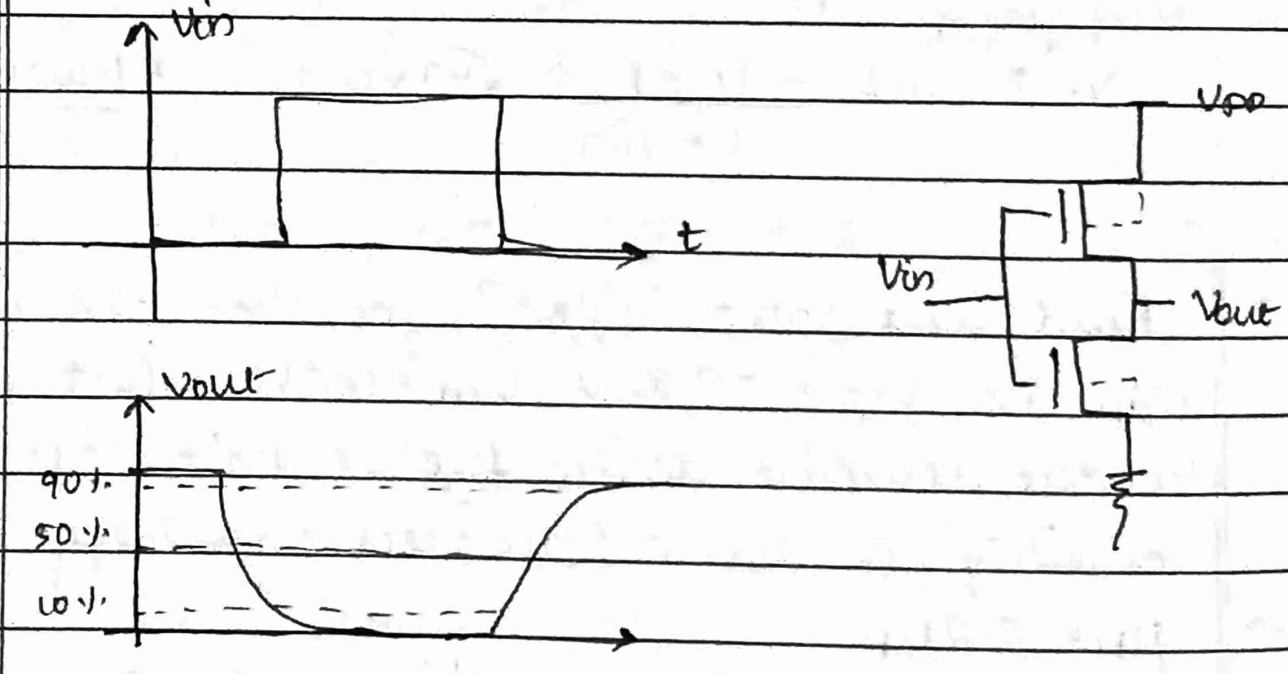
$$1.3 = \frac{3 - 0.82 + \sqrt{\beta_n/\beta_p}\ 0.6}{1 + \sqrt{\beta_n/\beta_p}}$$

$$1.3 + 1.3\sqrt{\frac{\beta_n}{\beta_p}} = 3 - 0.82 + \sqrt{\beta_n/\beta_p}\ 0.6.$$

$$(1.3 - 0.6)\sqrt{\frac{\beta_n}{\beta_p}} = 0.88.$$

$$\beta_n/\beta_p = 1.58.$$

Inverter Switching Characteristics



90% → 10% of Vout $t_f = t_{HL}$ fall time

10% → 90% of Vout $t_r = t_{LH}$ rise time

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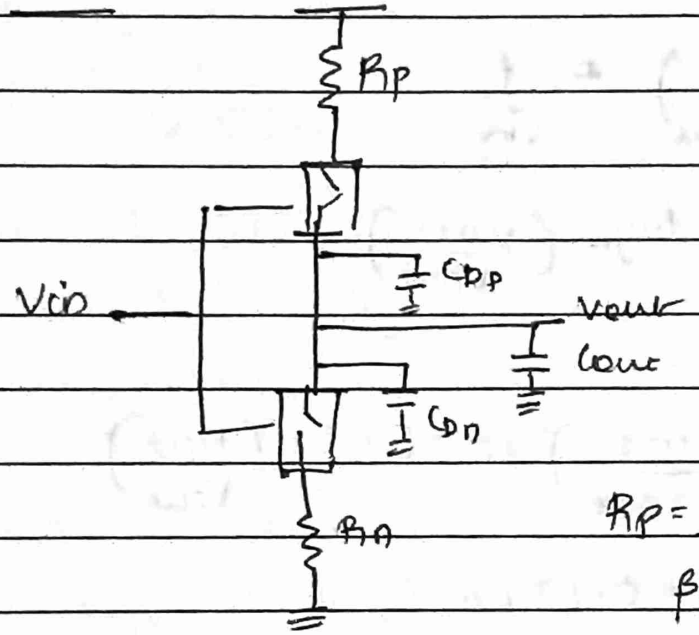
$f_{max} = \frac{1}{t_r + t_f}$ $\quad t_p = \frac{1}{t_r + t_f}$ (propagation delay)



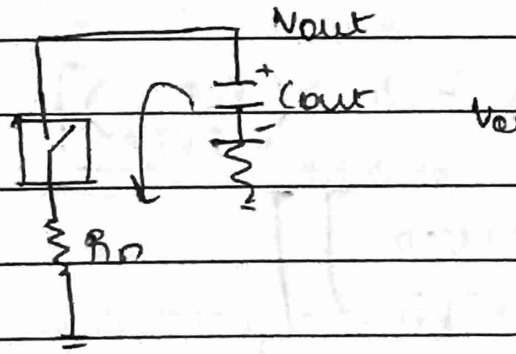
external cap

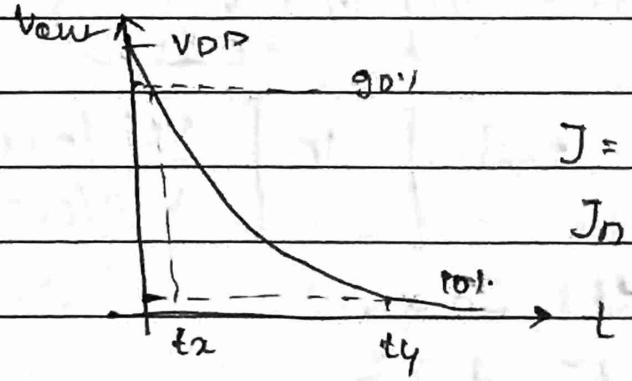
$C_{out} = C_{FET} + C_L$

$C_{FET} = C_{Dp} + C_{Dn}$

$R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)}$

$R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})}$





$J = RC$

$J_n = R_n C_{out}$

$i = -C_{out} \frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$

$V_{out}(t) = V_{DD}\, e^{-t/T_n}$

$T_n = R_n C_{out}$

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$$\frac{V_{out}}{V_{DD}} = e^{-t/\tau_n}$$

$$\log_n \frac{V_{out}}{V_{DD}} = \frac{-t}{\tau_n}$$

$$\log_n \left(\frac{V_{DD}}{V_{out}}\right) = \frac{t}{\tau_n}$$

$$t = \tau_n \log_n \left(\frac{V_{DD}}{V_{out}}\right)$$

$t_f = t_y - t_x$

$$t_f = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right) - \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$t_y \Rightarrow V_{out} = 0.1 V_{DD}$

$t_x \Rightarrow V_{out} = 0.9 V_{DD}$

$$t_f = \tau_n \left[\ln\left(\frac{V_{DD}}{0.1 V_{DD}}\right) - \ln\left(\frac{V_{DD}}{0.9 V_{DD}}\right) \right]$$

$$= \tau_n \left[\ln\left[\frac{V_{DD}/0.1 V_{DD}}{V_{DD}/0.9 V_{DD}} \right] \right]$$

$t_f = \tau_n \times 2.2$

$t_f = 2.2 \tau_n$

For rise time $\frac{V_{out}}{V_{DD}} = 1 - e^{-t/\tau_n}$

$t_r = 2.2 \tau_p$

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- Consider an inverter circuit that has FET aspect ratio of $(W/L)_n = 6$, $(W/L)_p = 8$, $K_n' = 150\mu A/V^2$, $K_p' = 62\mu A/V^2$, $V_{Tn} = 0.7V$, $V_{tp} = -0.85V$, $V_{DD} = 3.3V$, $C_{out} = 150fF$, $t_r = ?$, $t_f = ?$

→ $$R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)}$$

$$\beta_p = K_p' (W/L).$$
$$= 496\mu A/V^2.$$

$$R_p = \frac{1}{496\mu (3.3 - 0.85)} = 822.9\Omega$$

$$R_n = \frac{1}{150 \times 6 \times (3.3 - 0.7)} = 427.35\Omega$$

$t_r = 0.27$ nsec $= 2.2 R_p C_{out}$

$t_f = 0.141$ nsec $= 2.2 R_n C_{out}$

$f_{max} = 2.43$ GHz. $= 1/t_r + t_f$

- Find Midpoint voltage for the inverter for an external load of $C_L = 80fF$ is connected to output. The minimum channel length is $0.8\mu m$ & $C_{FET} = 50.45fF$. Also $W_p = 8\mu$, $W_n = 4\mu$. Find R_n, R_p, t_r, t_f, f_{max}

→

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→ $V_{tp} = -0.7V$, $V_{tn} = 0.6V$, $W_p = 8\mu m$, $W_n = 4\mu m$
$L = 0.8\mu m$, $K_n' = 150\mu A/V^2$, $K_p' = 60\mu A/V^2$
$V_{DD} = 5V$ $C_L = 80fF$ $C_{FET} = 50.45fF$.

→ $C_{out} = C_{FET} + C_L$
$= 80 + 50.45$
$= \underline{130fF}$.

$\beta_n = \left(\frac{W}{L}\right)_n K_n' = \frac{4\mu}{0.8\mu} \times 150\mu = 750\mu$

$R_n = \frac{1}{750\mu(5-0.6)} = 303.03\Omega$

$\beta_p = \left(\frac{W}{L}\right)_p K_p' = \frac{8}{0.8} \times 60\mu = 600\mu$

$= \frac{1}{600\mu(5-0.7)} = 387.59\Omega$

$t_r = 2.2(387.59)(130.45)f$
$= \underline{0.111 n Sec}$

$t_f = 2.2 \times 303 \times 130.45 \times f$
$= 0.869 n Sec$

$f_m = 1.0206 GHz$

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General Analysis of Gate.

$t_r = 2.2\ \tau_p$

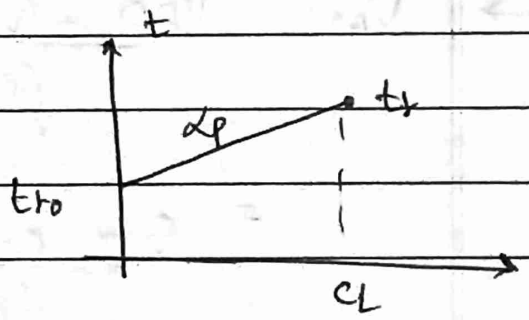
$= 2.2\ R_p C_{out}$

$t_f = 2.2\ \tau_n$

$= 2.2\ R_n C_{out}$

$t_r = 2.2\ R_p (C_L + C_{FET})$

$= 2.2\ R_p C_{FET} + \underbrace{2.2\ R_p C_L}_{\alpha_p}$



if $C_L = 0$

$t_{r0} = 2.2\ R_p C_{FET}$

else

$t_r = 2.2 R_p C_{FET} + \alpha_p C_L$

$= t_{r0} + \alpha_p C_L$

$\alpha_p = 2.2\ R_p = 2.2 \dfrac{1}{\beta_p (V_{DD} - |V_{tp}|)} = \dfrac{2.2}{k_p' (W/L)_p (V_{DD} - |V_{tp}|)}$

$\downarrow \alpha_p \propto \dfrac{1}{(W/L)_p} \uparrow$

For fall & rise time to be less, i.e. S/m to be faster area must be compromised.

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○ An inverter uses FET with $\beta_n = 2.1\ mA/V^2$, $\beta_p = 1.8\ mA/V^2$, $V_{tn} = 0.6V$, $V_{tp} = -0.7V$, $V_{DD} = 5V$. The parasitic FET capacitance at output node is estimated to be $C_{FET} = 74fF$.

i) Find mid point voltage V_m

ii) Find R_p, R_n. Calculate t_r & t_f at $C_L = 0$

iii) Calculate t_r & t_f at the output $C_L = 115fF$

iv) Plot t_r & t_f as fn of C_L

→ $$V_M = \frac{V_{DD} - |V_{tp}| + \sqrt{\beta_n/\beta_p}\, V_{tn}}{\sqrt{\beta_n/\beta_p} + 1}$$

$$= \frac{5 - 0.7 + \sqrt{2.1/1.8} \times 0.6V}{\sqrt{2.1/1.8} + 1}$$

$$= \frac{4.94}{\sqrt{\frac{2.1}{1.8}} + 1} = 2.37V$$

ii) $$R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)} = \frac{1}{1.8m(5 - 0.7)} = 129.2\Omega$$

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})} = \frac{1}{2.1m(5 - 0.6)}$$

$$= 108.22\Omega$$

$\alpha_p = 284.218$ $\alpha_n = 238.084$.

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— $t_r = 2.2 \times R_p \, C_{out}$

$= 2.2 \times 129.19 \times 74 \times 10^{-15}$

$= \underline{0.0210 \text{ nsec}}$

$t_f = 2.2 \times R_n \, C_{out}$

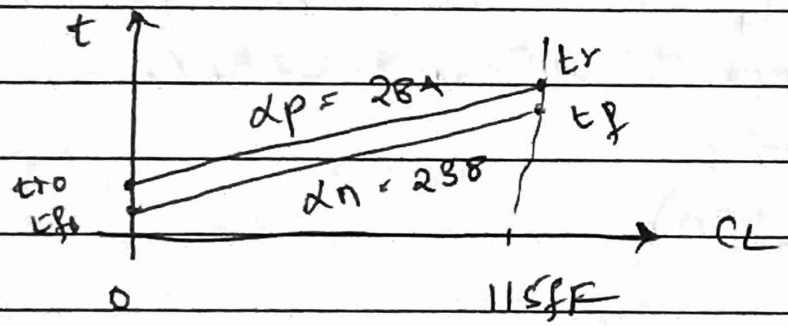
$= \underline{0.0176 \text{ nsec}}$

— $t_r = 2.2 \times R_p \, C_{out}$

$= 2.2 * 129.19 \times (74 + 115) \times 10^{-15}$

$= \underline{0.0537 \text{ nsec}}$

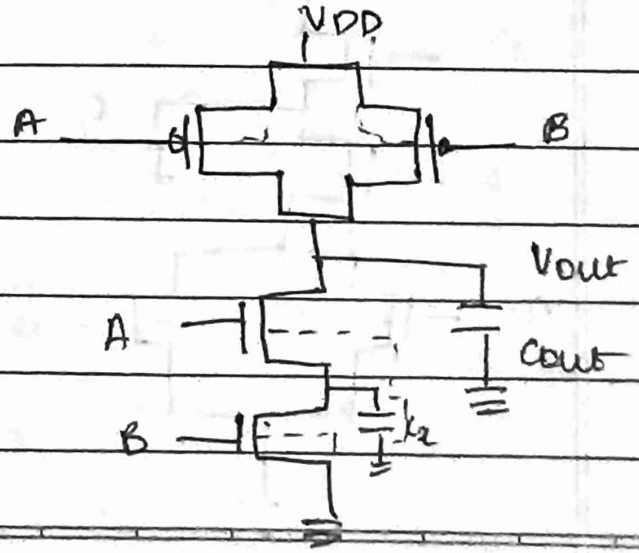
$t_f = 0.0449 \text{ nsec}$



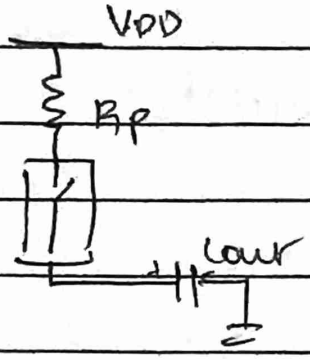
Transient Analysis.

— NAND Gate.

$Y = \overline{A \cdot B}$



Worst Case: A/B is ON

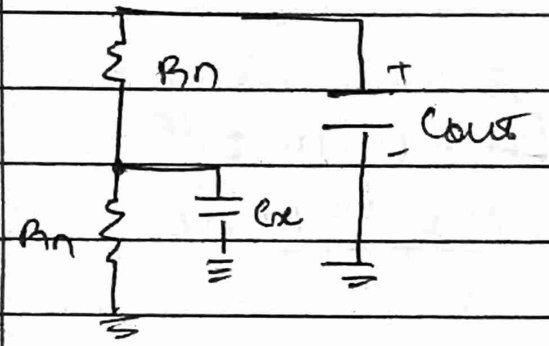


$t_r = 2.2 R_p C_{out}$

$= 2.2 R_p (C_{FET} + C_L)$

$t_r = t_{ro} + \alpha_p C_L$

$\alpha_p = 2.2 R_p$



$I_{n_1} = 2 R_n C_{out}$

$I_{n_2} = R_n C_x$

$I_n = I_{n_1} + I_{n_2}$

$t_f = 2.2 I_n$

$= 2.2 (2 R_n C_{out} + R_n C_x)$

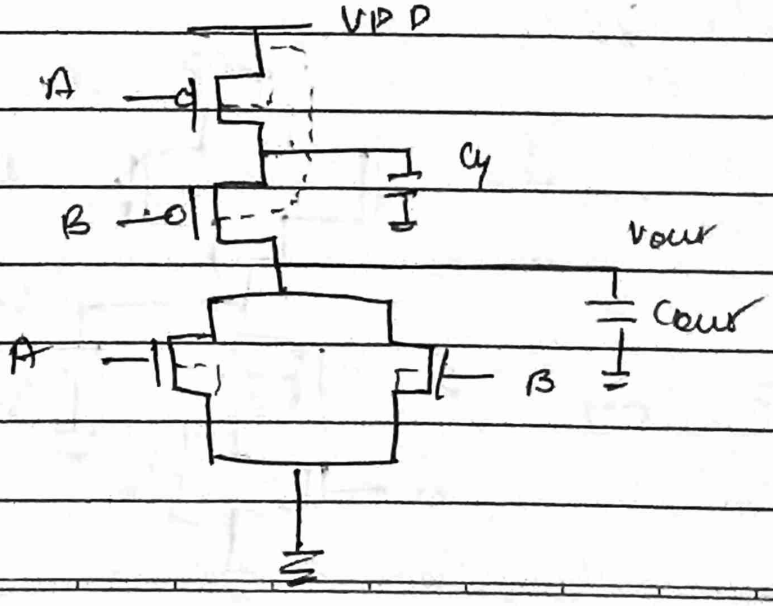
$t_f = 2.2 (2 R_n (C_{FET} + C_L) + R_n C_x)$

$= 4.4 R_n C_{FET} + 4.4 R_n C_L + 2.2 R_n C_x$

$\alpha_n = 4.4 R_n$

$= 2(2.2 R_n)$

NOR Gate



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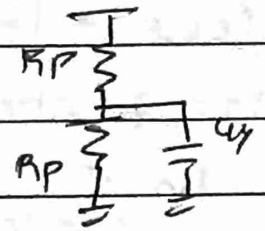
$T_{rF} = 2.2 R_p C_4$

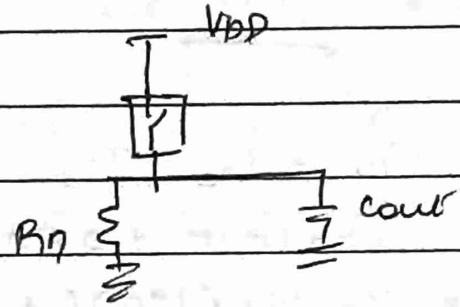
$T_{R_2} = 2 \times 2.2 R_p C_{out}$

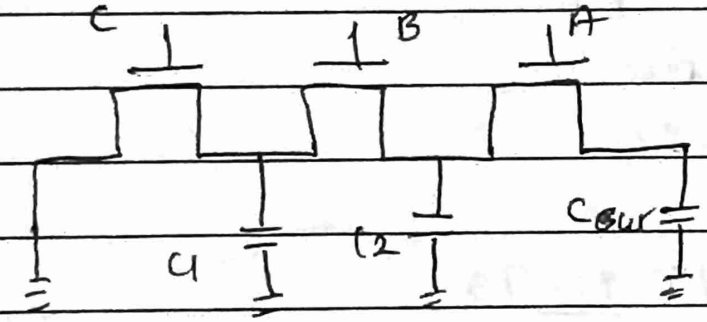
$t_r = 4.4 R_p C_{out} + 2.2 R_p C_4$

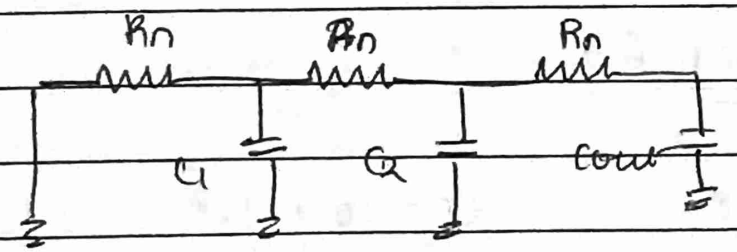
$\alpha = 4.4 R_p.$



$t_f = 2.2 R_n C_{out}$







Find discharge time constant from $C_{out} = 130fF$ using the I-MOOre formulae for above CKT. Also find T if we ignore C_1 & C_2, what is the % error introduced.

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— $C_{out} = 130fF$ $C_1 = 36fF$, $C_2 = 36fF$, $V_{DD} = 3.3V$

$\beta_n = 2mA/V^2$, $V_{tn} = 0.7V$, $T_n = R_n \cdot C_{out}$

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})}$$

$$R_n = \underline{192.3\Omega}$$

$T_n = T_{n1} + T_{n2} + T_{n3}$

$= 3R_n C_{out} + 2R_n \cdot C_2 + R_n C_1$

$= 3 \times 192 (130)f + 2 \times 192 (36f) + 192 \times (36)f$

$= 95.77 psec.$

$T_n = 3R_n C_{out}$

$T_n = 75 psec$

$$\% Error = \frac{95.77 - 75}{95.77}$$

$$= \underline{21.63.}$$

— $t_r = 90\% \cdot 1.8$ $\quad t_f = 10\% \cdot 1.8$

$= 1.62$ $\quad = 0.18$

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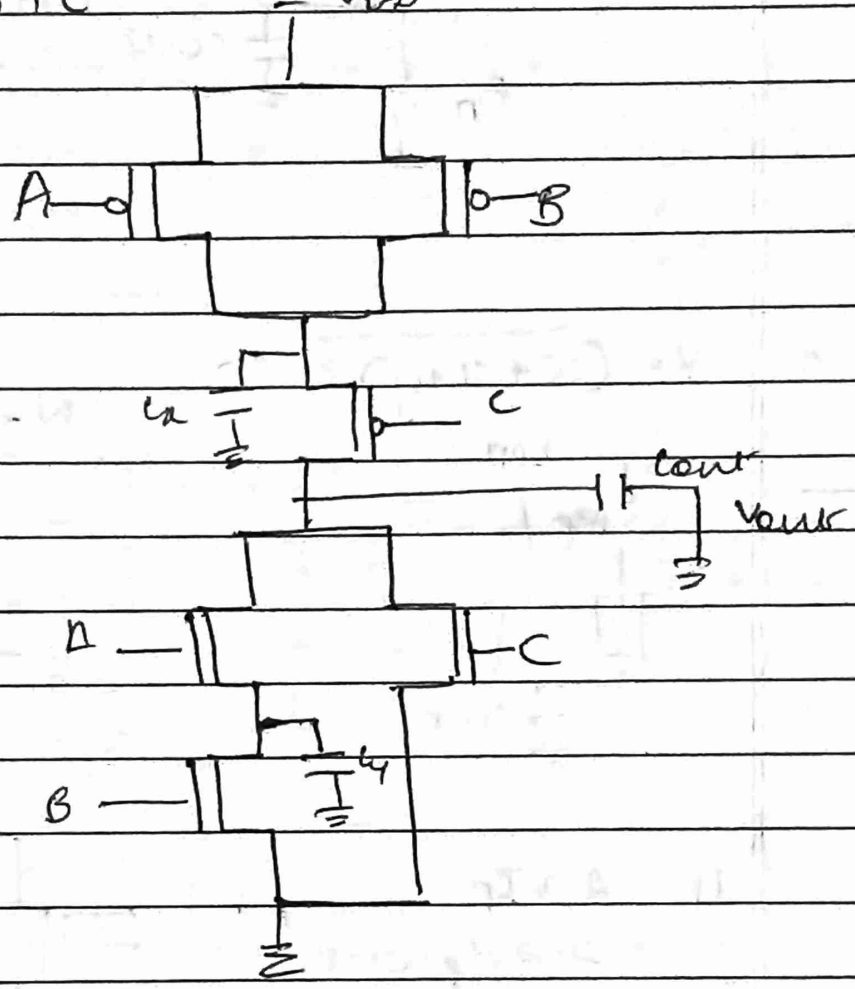
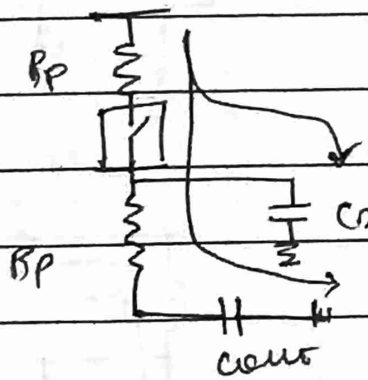
For $Y = \overline{A \cdot B + C}$



Worst case condn: Either A or B must be on & C must be always on (rise time)



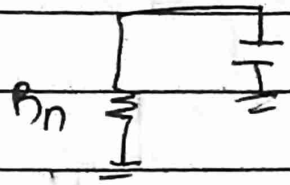
$T_{n} = 2.2\ R_p C_x$

$T_{n2} = 2.2\ (2R_p)\ C_{out}$

$t_r = 2.2 R_p C_x + 4.4 R_p C_{out}$

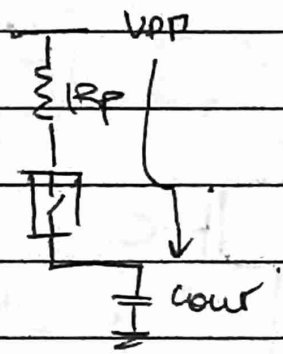
$\alpha = 4.4 R_p$

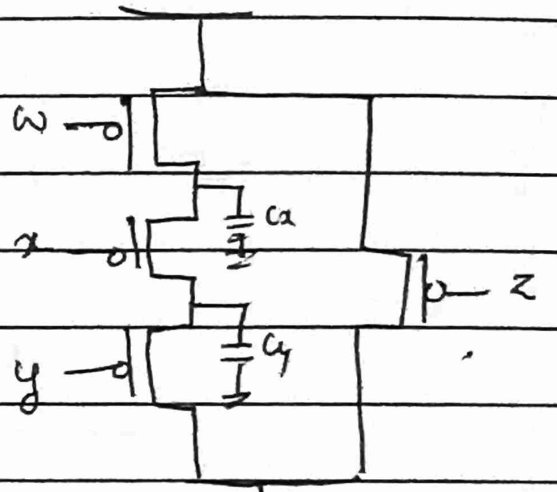
Worst case (fall time): Either C must be on or both A & B must be on



$t_f = 2.2 R_n C_{out}$

$Y = \overline{(W + X + Y) Z}$

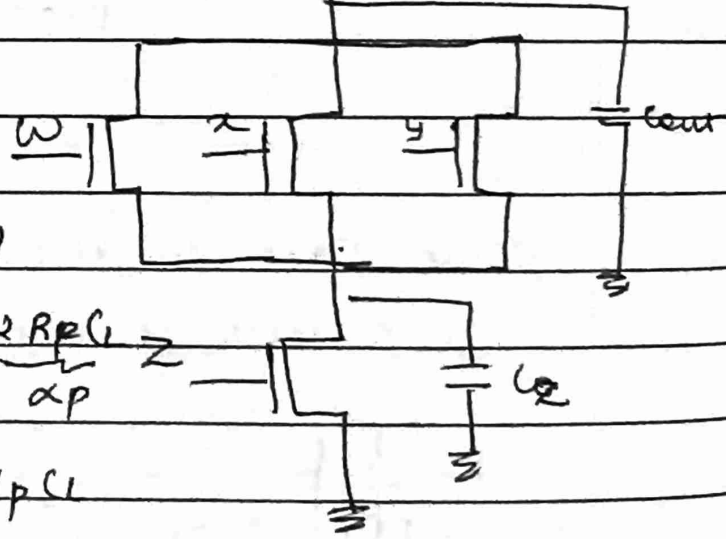




$t_r = 2.2 R_p C_{out}$

$= 2.2 R_p (C_{FET} + C_L)$

$C_{out} = 2.2 R_p C_{FET} + \underbrace{2.2 R_p C_L}_{\alpha_p}$



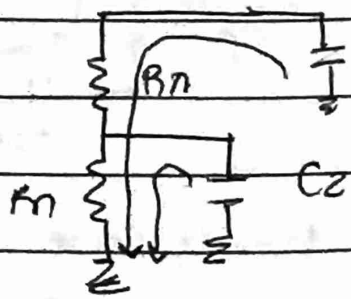
$t_r = 2.2 R_p (C_{FET}) + \alpha_p C_L$

$\alpha_p = 2.2 R_p$

$t_f = 2.2 C_n$

$T_{n1} = 2 R_n C_{out}$

$T_{n2} = R_n C_2$



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$t_f = 2.2\ (\tau_{n1} + \tau_{n2})$

$t_f = 2.2\ (2R_n(C_{FET} + C_L) + R_n C_2)$.

$t_f = 2.2R_n\ (2C_{FET} + C_2) + 4.4\ R_n C_2$

$\alpha_n = 4.4R_n$

$\alpha_n = 2\ (2.2\ R_n)$.

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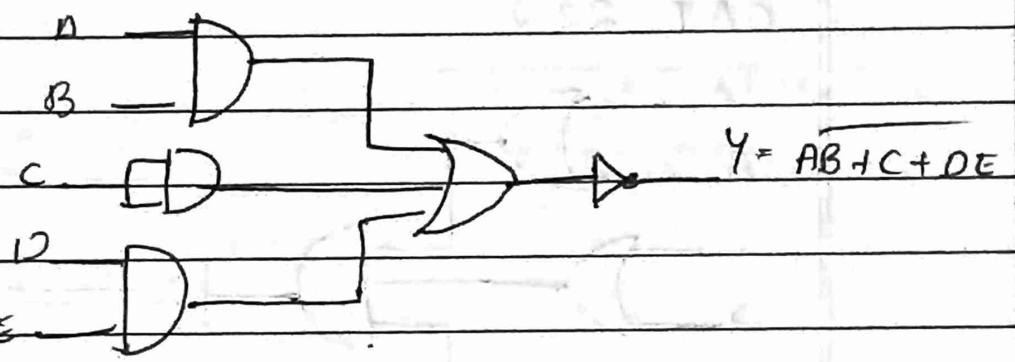

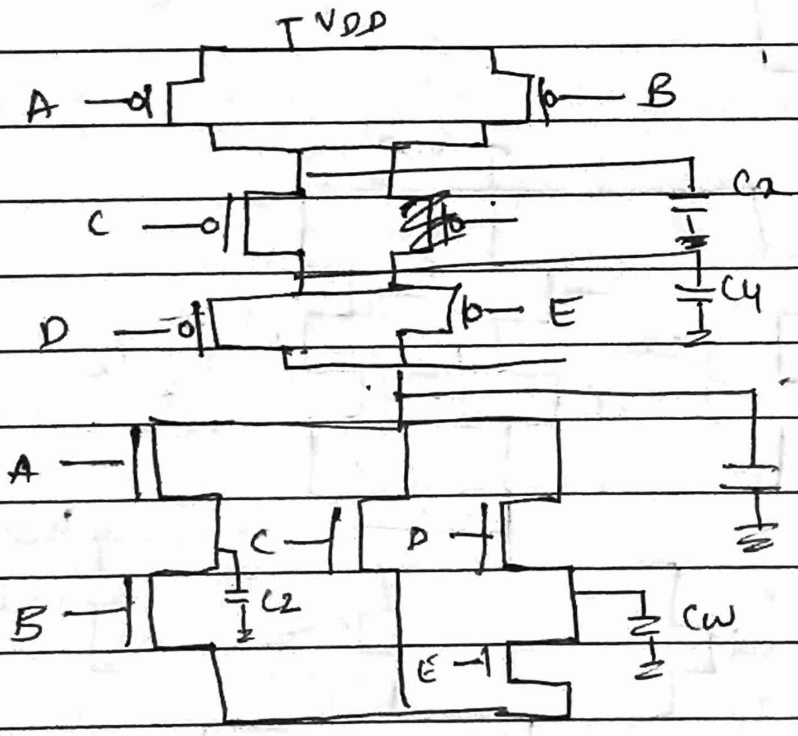

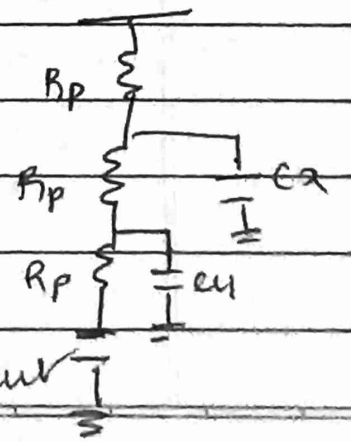

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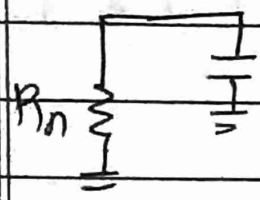
$t_r = 2.2(3R_p(C_{FET}) + 2.2 \times 3R_p C_L + 2.2 \times 2R_p \times C_4 + 2.2R_p C_x$



$t_f = 2.2 R_n C_{out}$.

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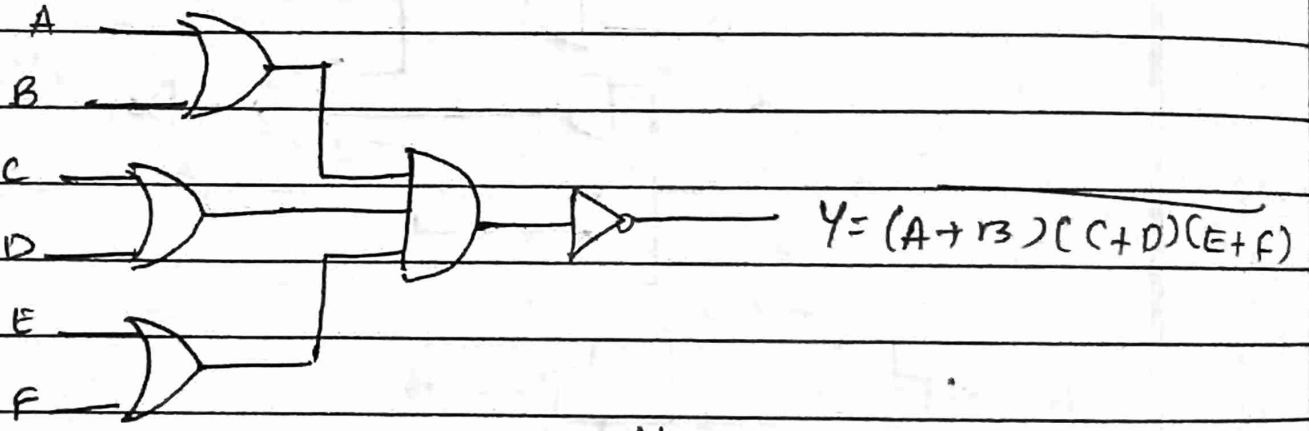
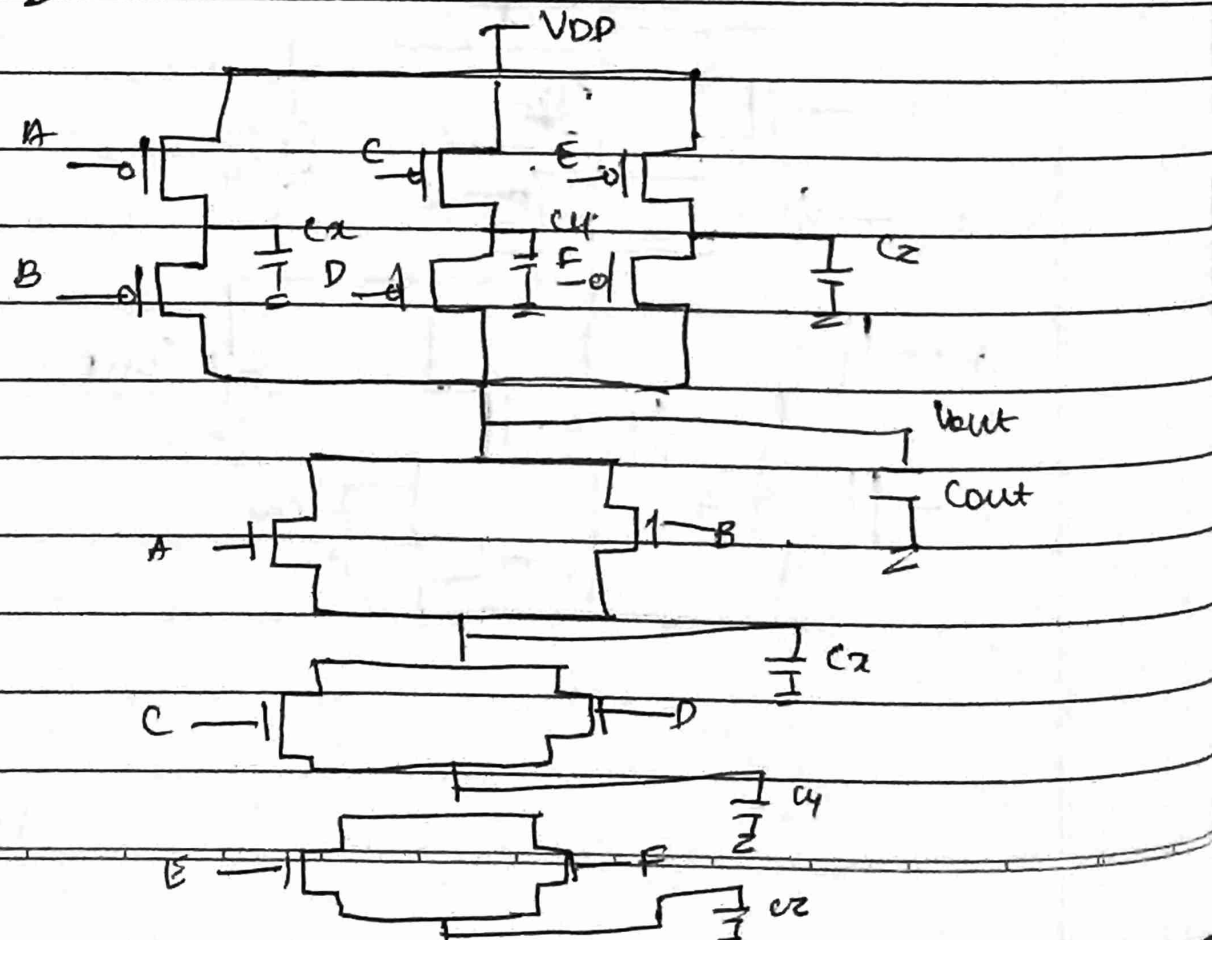
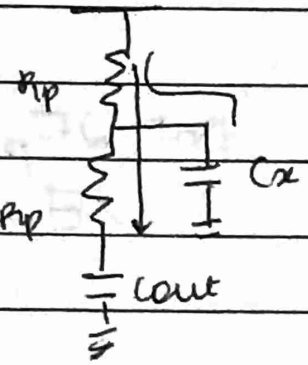
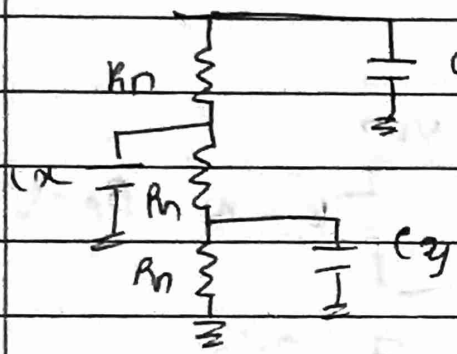




$t_r = 2.2 R_p C_x + 2.2 R_p (2 C_{out})$



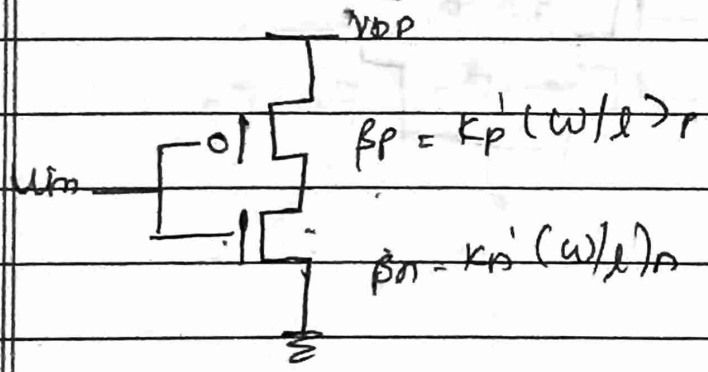
$= 2.2 R_p C_x + 4.4 R_p C_{FET} + 4.4 R_p C_L$

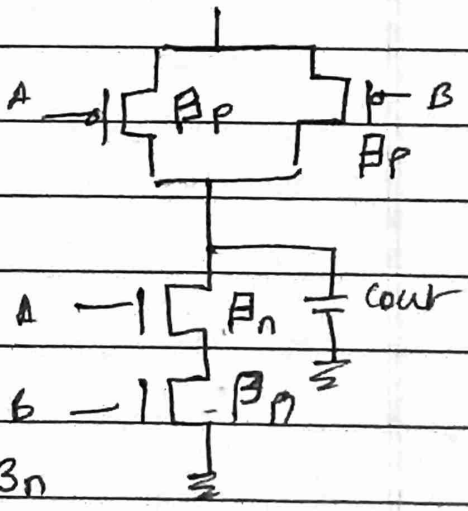


$t_f = 2.2 R_n C_y + 2.2 (2R_n) C_x + 2.2 (3R_n) C_{FET} + 2.2 (3R_n) C_L$

Gate delay for Transient Performance.

$Y = \overline{A \cdot B}$





$\beta_n = k_n' (W/L)_n$

$R_n = \frac{1}{\beta_n [V_{DD} - V_{tn}]}$

$R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})}$

$\beta_n = 2\beta_n$

Since $2R_n = R_n$

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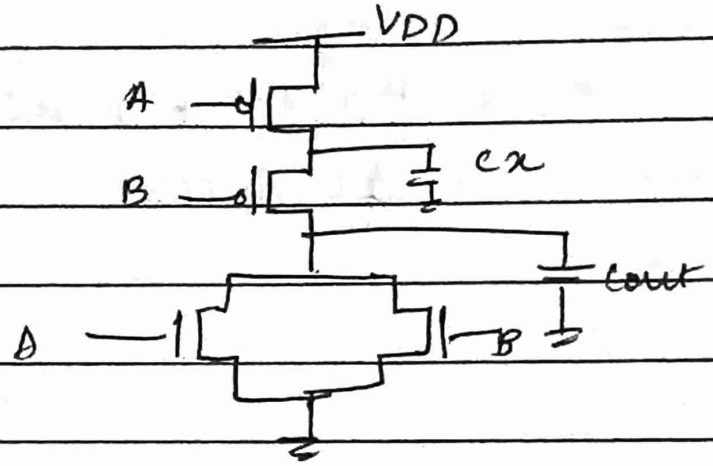
NOR Gate: $\overline{A+B} = Y$



$2p \parallel 2R_p = R_p$

$2\beta_p = 2\beta_p$

0. $Y = \overline{AB+C}$