MOSFET Device & its characteristics

FET (Field effect transistor)

- JFET
- MOSFET's
  - depletion-type MOSFET
    - n-channel dep. typ
    - p-channel
  - enhancement type MOSFET
    - n-chamel
    - p-channel
- MESFET

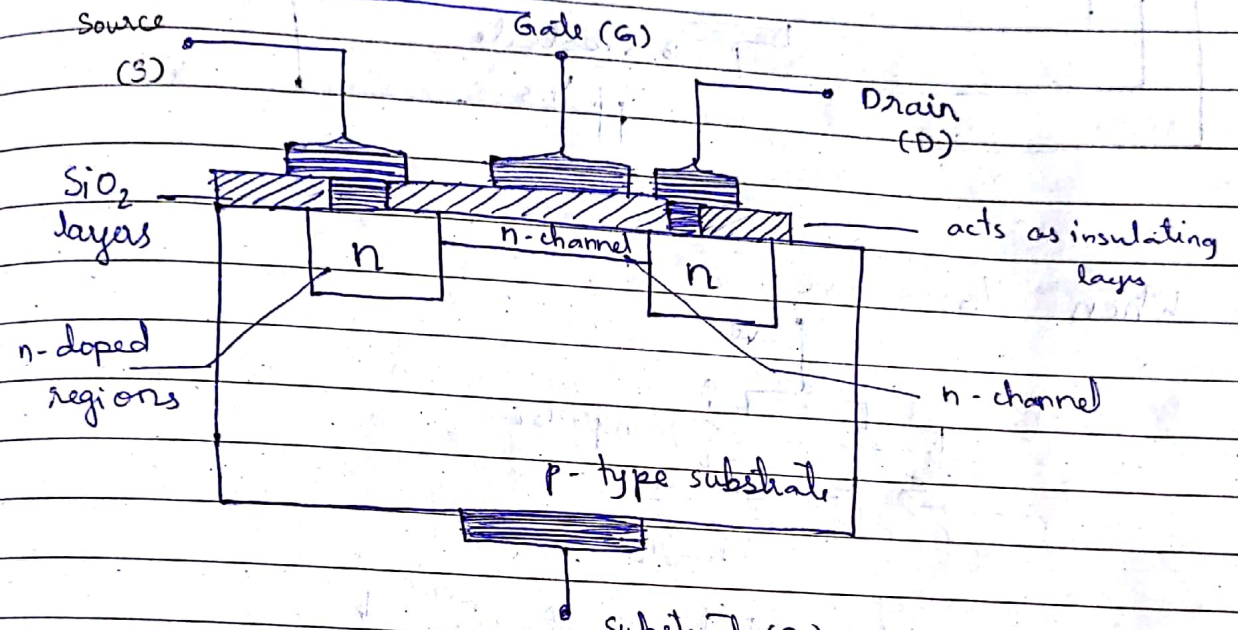
BJT	MOSFET
Current controlled	Voltage controlled
Bipolar (2 types of charge carries for current cond.)	Unipolar devices
Comp. less	High input impedence
AC voltage gain for BJT amplifies is higher.	Comp. less
	Temp. stability is high
	* Smaller in size

Since smaller in size & easy manufacturing it is popular.

n-channel depletion type

MOSFET

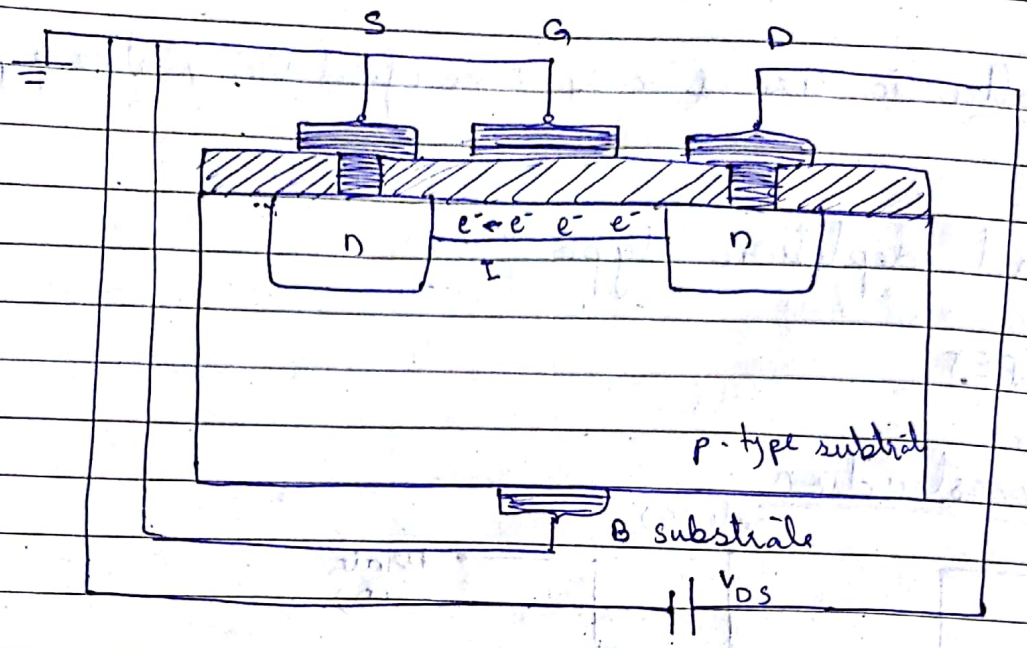
Basic Construction :-



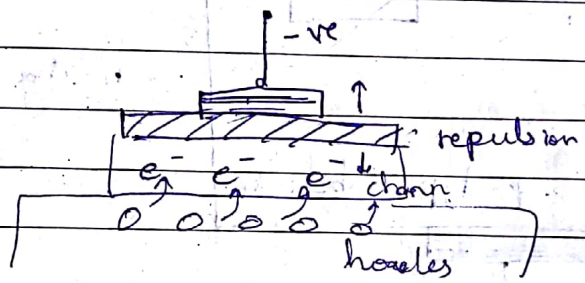
- Due to SiO_2 layer, its i/p impedance, so the gate current is '0'.

Basic Operation and its characteristics

(i) $V_{GS} = 0V$, V_{DS} = +ve voltage.



(ii) When V_{GS} = - ve



So total no. of $e^{\ominus}$ ↓

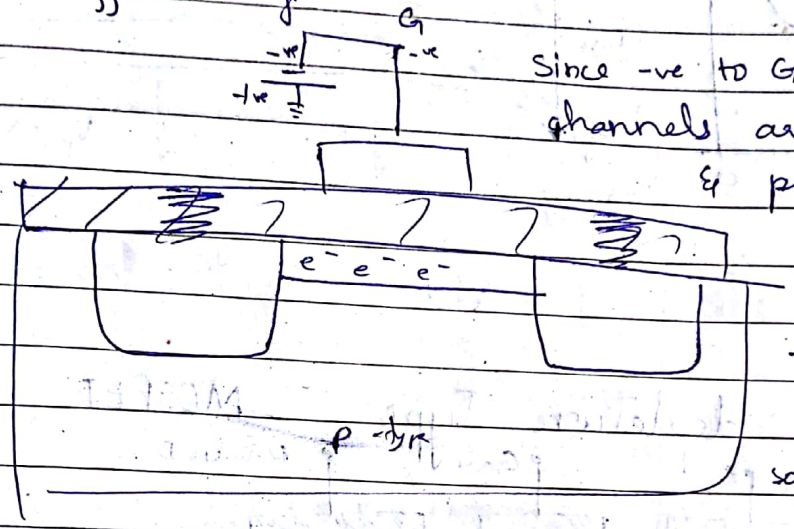
So current also decreases

When a -ve voltage is applied across there is repulsion in the n-channel of $e^{\ominus}$, so the holes present in p type holes undergo recombination, so $e^{\ominus}$ no. ↓, So current ↓.

(iii) When V_{GS} : +ve

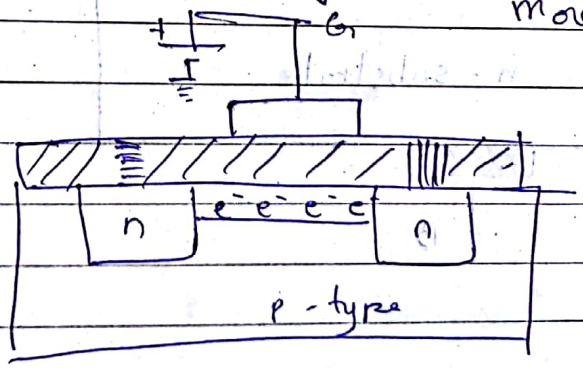
I_D ↑

(i) Pinch off voltage: The voltage of V_G at which the drain current I_D becomes zero is called pinch off voltage



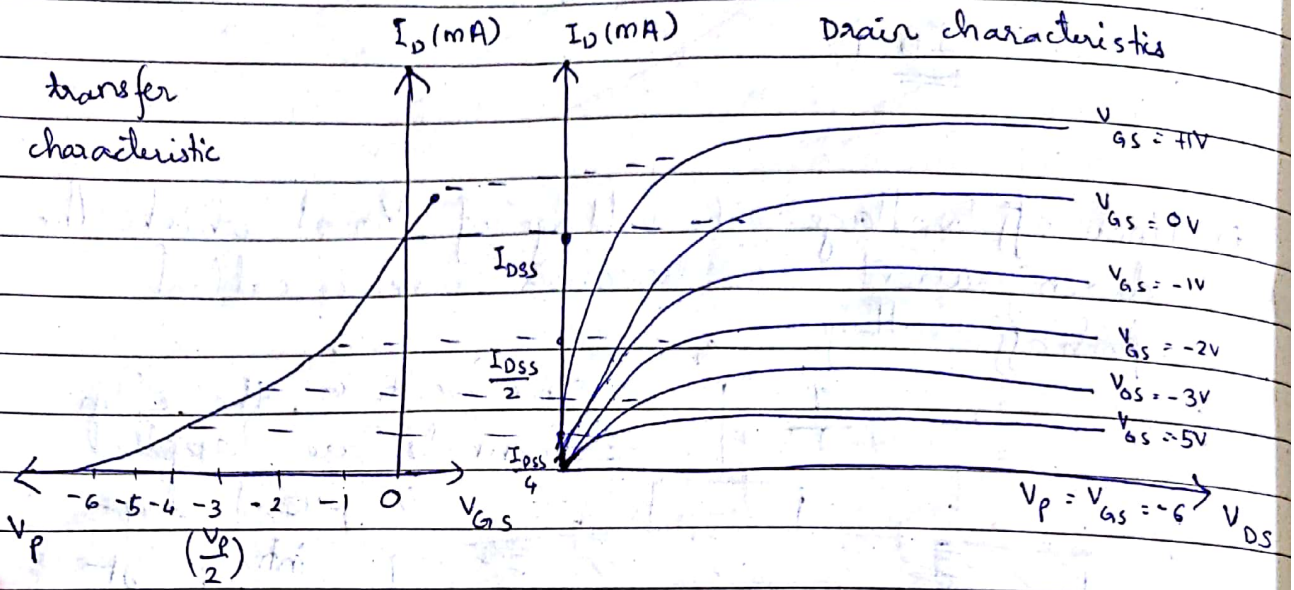
Since -ve to G, the $e^{\ominus}$ in channels are repelled & pused deeper into p-type & undergo recombi till a stage ∃ all $e^{\ominus}$ are combined so. $I_D = 0$

(ii) When +ve voltage across G

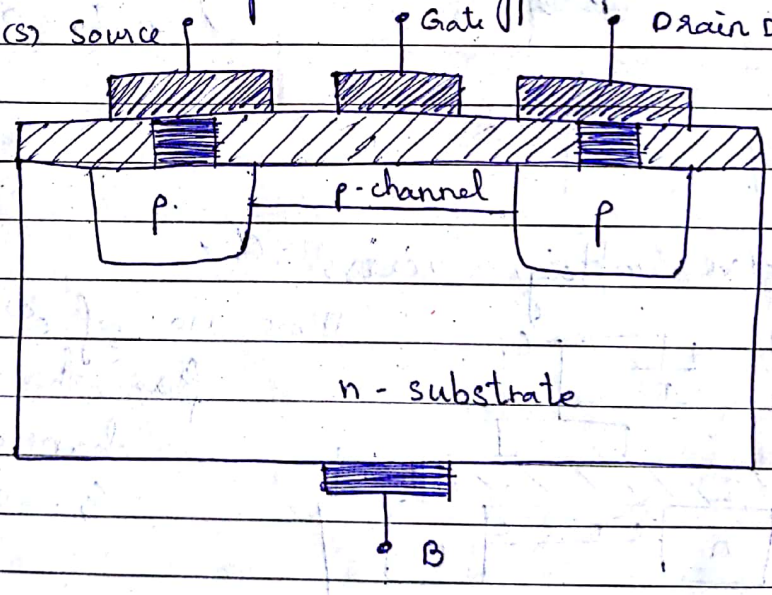


more no. of $e^{\ominus}$ will flow through channel & I_D ↑.

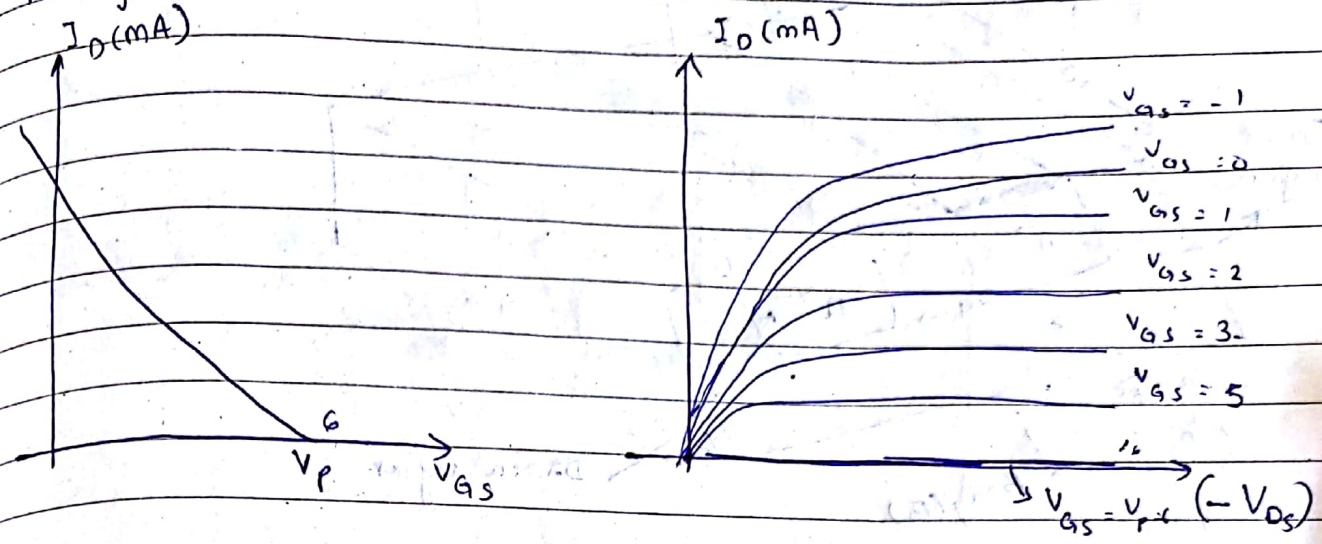
Transfer and drain characteristics



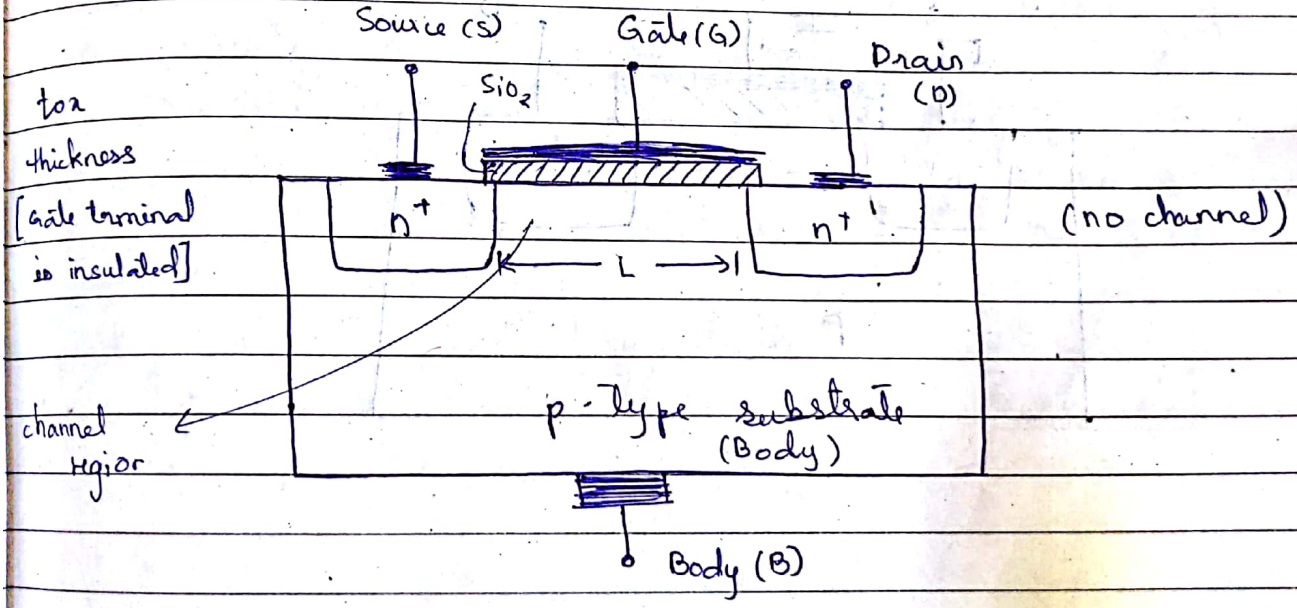
p-channel depletion type MOSFET



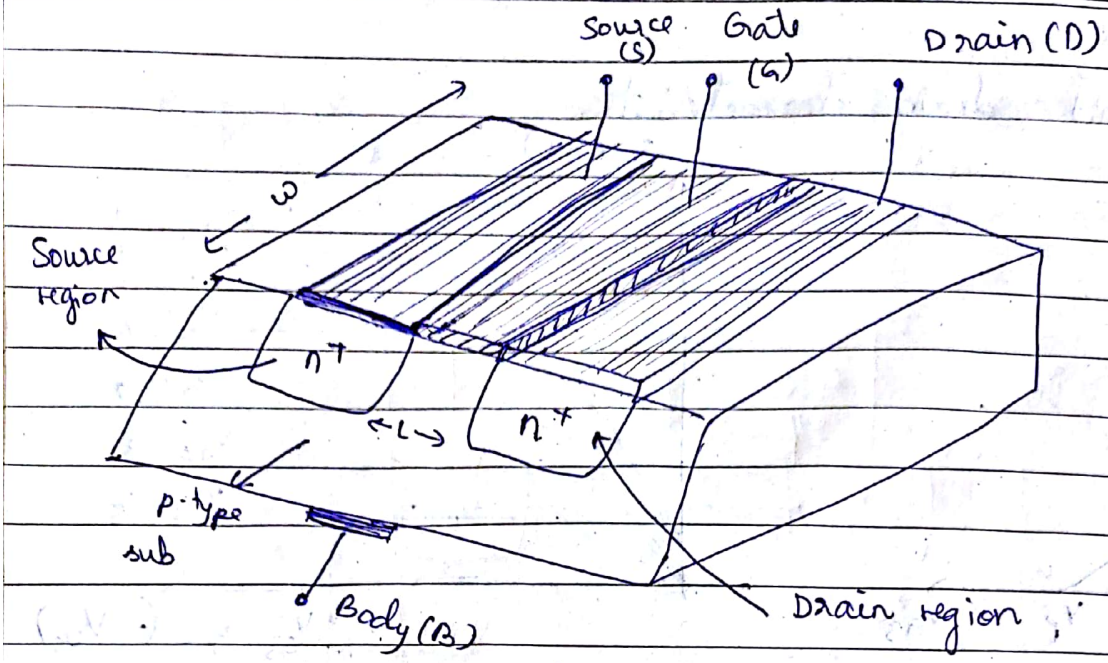
Transfer and drain characteristic



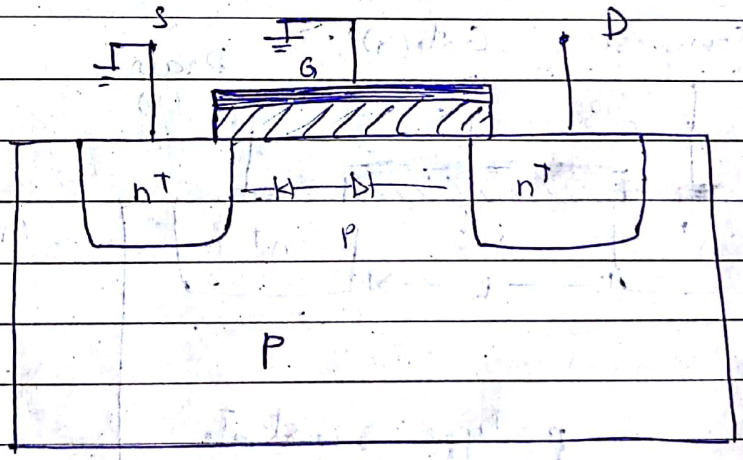
Enhancement type n-channel MOSFET



IGFET (Insulated Gate)

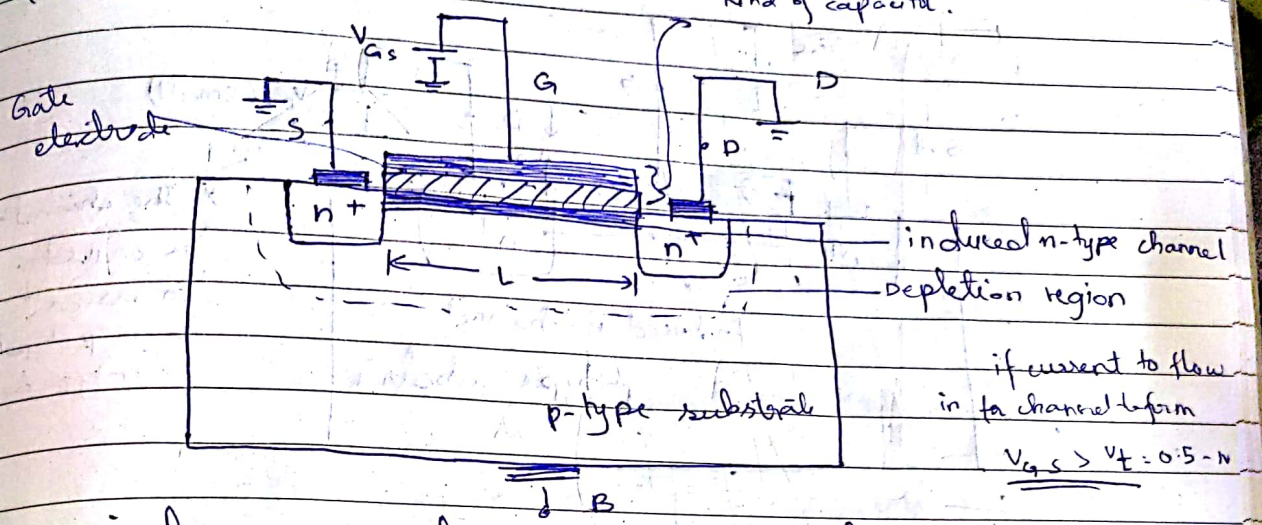


1) Operation with no gate :- ($V_{GS} = 0$, $V_{DS} = 0$ / +ve)



2) Creating a channel for current flow:

($V_{GS} = V_t$) ($V_{DS} = 0V$)



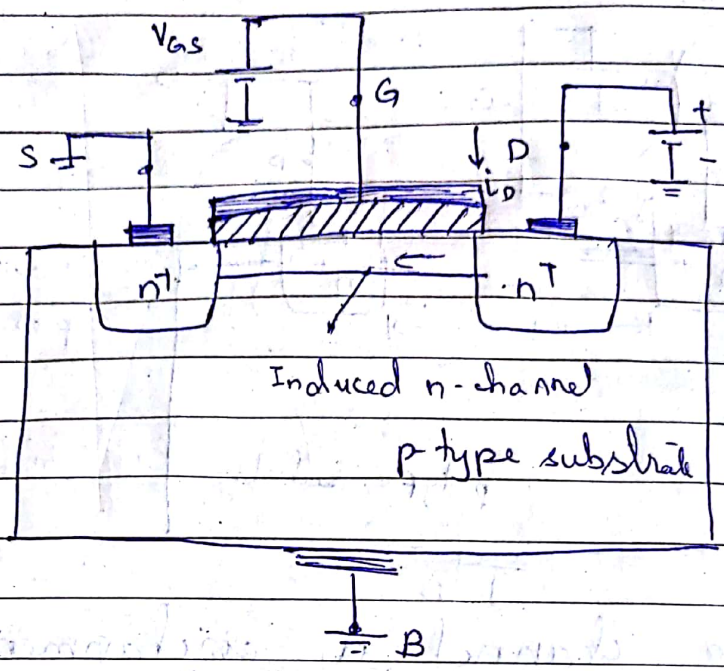
if current to flow in the channel to form $V_{GS} > V_t : 0.5 - 1V$

To induce a channel in enchanment type, we apply a +ve V_{GS} so that the holes present in p-type are pushed inside, so we a have a region of acceptor ions in the depletion region. Due the -ve V_{GS} the n-type are attracted & a channel of -ve $e^{\ominus}$, That V_{GS} voltage at which the channel is formed is called threshold voltage. (V_t)

Ily for p n-type substrate, a -ve V_{GS} is given

③ Applying a small V_{DS} ($V_{GS} > V_t$)

(V_{DS} = small +ve voltage)



* The channel here is called as inversion layer as in p-type a n-type channel

Now applying + V_{DS}, $e^{\ominus}$ from channel flow from S to D., so we have current flow from D to S (i_D) provided $V_{GS} > V_t$

* Greater the value of V_{GS}, more $e^{\ominus}$ get attracted towards V_{GS}, $\ominus \uparrow$ so channel dept with increase, so conductance will increase & resistance will decrease.

So for more current to flow the excess gate voltage is applied given by overdrive voltage

| excess gate volt = $V_{GS} - V_t$ |

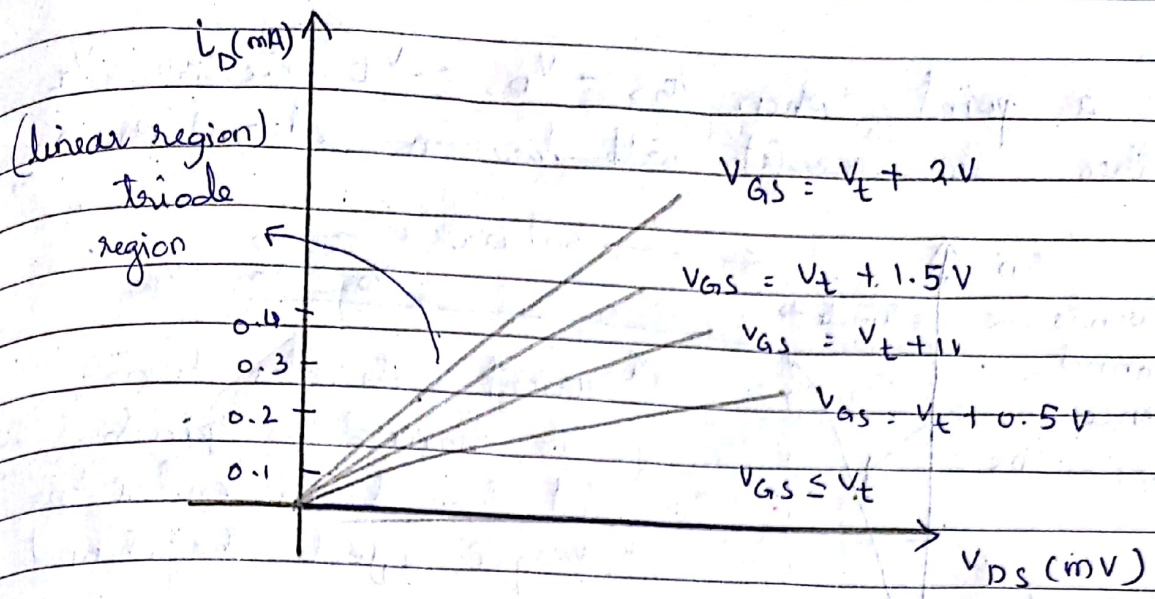
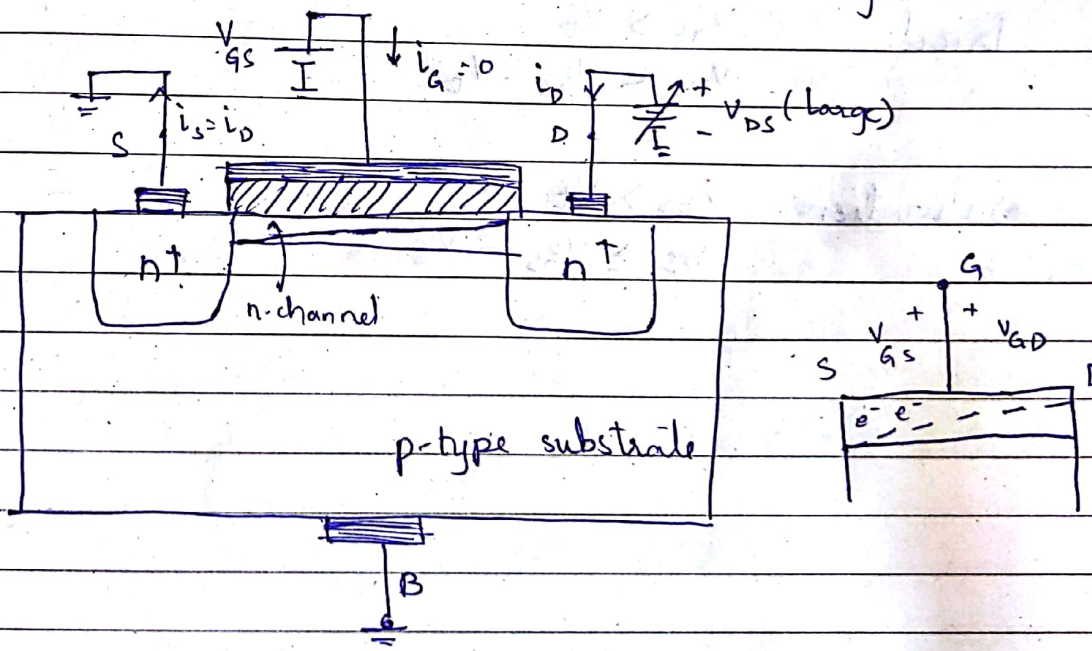


fig: When a small amount of V_{DS}

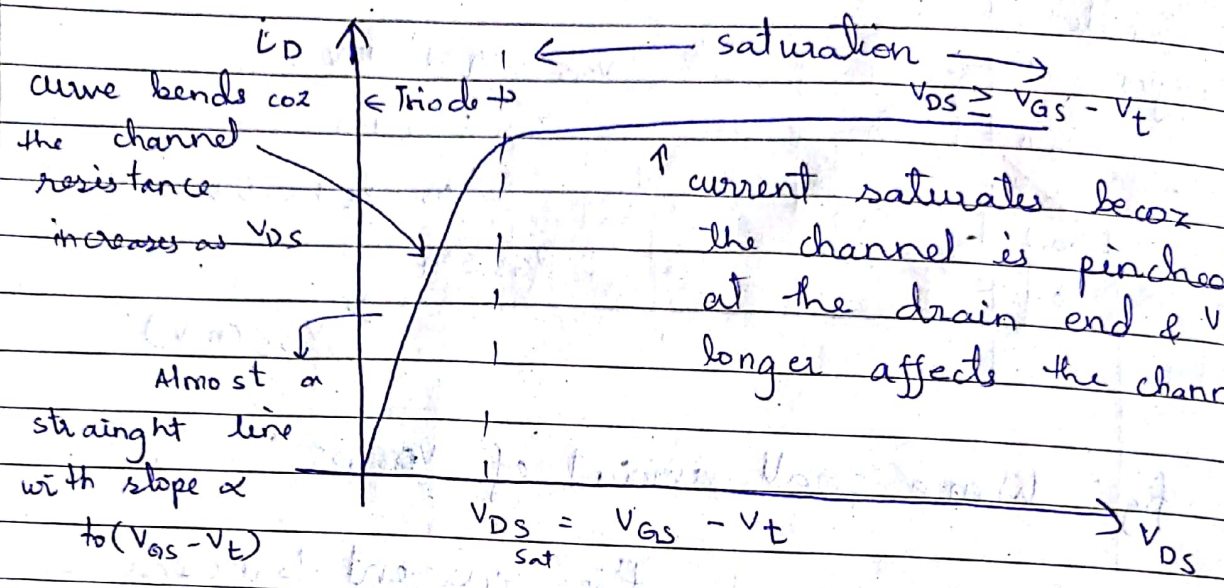
* V_{GS} has to increase for the current to increase or enhance, so it is called enhancement type MOSFET

4) Operation as V_{DS} is increased (V_{DS} = larger +ve voltage)



The channel depth tappers, w.r.t, the voltage is 0 but at D, as V_{DS} is ↑, $V_{GD} = V_{GS} - V_{DS}$, so V_{GD} ↓, so due to lower potential, so we have a narrow channel as less no. of e^- are attracted

At a point when $V_{GS} - V_{DS} = V_t$ i.e $V_{GD} = V_t$ then the mosfet will be in saturation region.



Cutoff $V_{GS} < V_t$

Triode $V_{GS} > V_t$

$V_{DS} < V_{GS} - V_t$

Saturation $V_{GS} > V_t$

$V_{DS} \geq V_{GS} - V_t$

Derivation of drain current I_D in linear region & saturation region for n-channel enhancement type MOSFET

→ Let t_{ox} thickness of oxide layer
→ Let C_{ox} be capacitance of

$$\varepsilon_r = \frac{\varepsilon}{\varepsilon_0}$$

Let ε_{ox} be permitivity of oxide layer

$$\varepsilon_{ox} = \varepsilon_{SiO_2} \varepsilon_0 \quad \text{——— (1)}$$

$$i = \frac{dq}{dt} \quad \text{——— (2)}$$

So Drain current $I_D = \frac{Q_c}{T_{SD}}$

2 Electric fields

Horizontal	Source Drain
Vertical	due to gate

where Q_c - charge induced in the channel
T_{SD} - electron transit time from S - Drain

General eq for time is $T_{SD} = \frac{L}{V}$ — channel length
V — velocity of $e^\ominus$

$$V = \mu_n E_{DS} \quad \text{——— (4)}$$

where μ_n = $e^\ominus$ mobility

E_{DS} = electric field b/n drain & source

$$E_{DS} = \frac{V_{DS}}{L} \quad \text{——— (5)}$$

Substitute eqn (5) in eq. (4)

$$v = \frac{\mu_n V_{DS}}{L} \quad \text{——— (6)}$$

Substitute eq. (6) in (3)

$$\boxed{I_{SD} = \frac{L^2}{\mu_n V_{DS}}} \quad \text{——— (7)}$$

Substitute (7) in (2)

$$I_D = \frac{Q_S \cdot \mu_n V_{DS}}{L^2} \quad \text{——— (8)}$$

In triode region $V_{DS} < V_{GS} - V_t$

Charge per unit area $= \varepsilon_o E_G$ ——— (9)

where E_G - electric field at the gate, hence induced charge Q_c can be written as $\varepsilon_o E_G \times (W \times L)$ ——— (10)

$$E_G = \frac{\text{voltage}}{\text{length}} = \frac{(V_{GS} - V_t) - V_{DS}/2}{t_{ox}} \quad \text{——— (11)}$$

Subt. (11) in (10)

Capacitance

$$Q_C = \frac{\varepsilon_0 \times W \times L}{t_{ox}} \times \left[(V_{GS} - V_t) - V_{DS}/2 \right]$$

$$Q_C = C_{ox} W L \left[(V_{GS} - V_t) - V_{DS}/2 \right] \quad \text{--- (12)}$$

Subt. (12) in (8)

$$I_D = C_{ox} \cdot W \frac{\left[(V_{GS} - V_t) - V_{DS}/2 \right]}{L} \mu_n V_{DS}$$

In sat. region

$$V_{DS} = V_{GS} - V_t$$

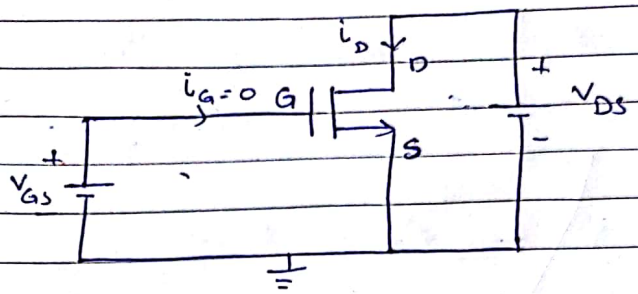
$$\therefore \quad I_D = C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_t) - \frac{V_{GS} - V_t}{2} \right] \mu_n V_{DS}$$

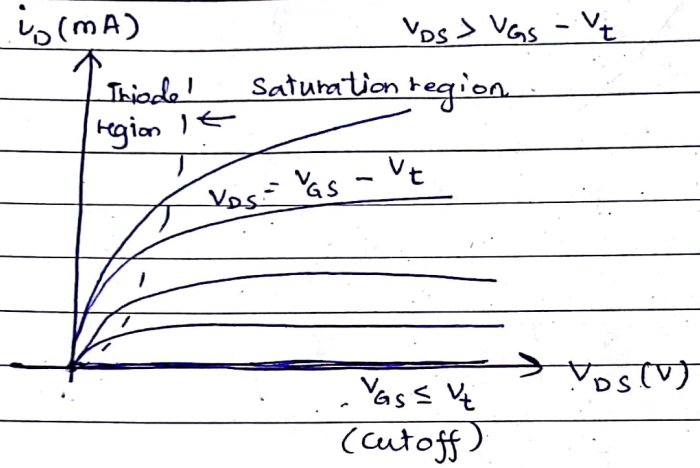
$$I_D = \mu_n C_{ox} \left(\frac{W}{L} \right) \left[\frac{1}{2} (V_{GS} - V_t)^2 \right]$$

as

(11)

The $i_D - V_{DS}$ characteristics





Cutoff

$V_{GS} < V_t$

Triode

$V_{GS} \geq V_t$

$\boxed{V_{DS} < V_{GS} - V_t}$

$$i_D = K_n' \left(\frac{W}{L}\right) \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$i_D = k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t) V_{DS}$$

So it behaves as linear resistance r_{DS}

$$r_{DS} = \left.\frac{V_{DS}}{i_D}\right|_{V_{GS} = V_{GS}\ (\text{same value})}$$

$$r_{DS} = \frac{1}{\left[k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)\right]}$$

So it will behave as resistance in triode region.

$$V_{GS} - V_t = V_{ov} \quad (\text{overdrive})$$

$$\boxed{r_{DS} = \frac{1}{k_n' \frac{W}{L} \cdot (V_{ov})}}$$

Saturation

There has to be a channel formed with $V_{GS} \geq V_t$

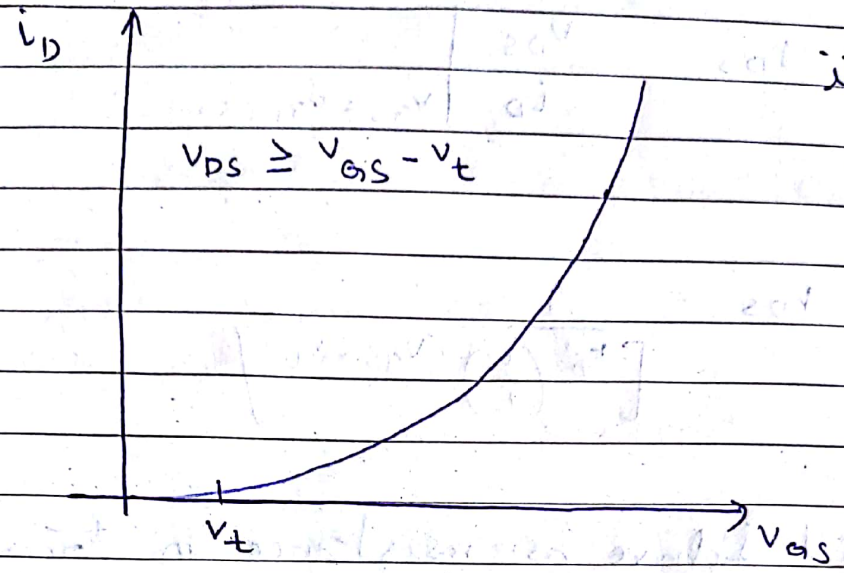
$$V_{GD} \leq V_t$$

$$V_{GS} - V_{DS} \leq V_t$$

$$\boxed{V_{DS} \geq V_{GS} - V_t}$$

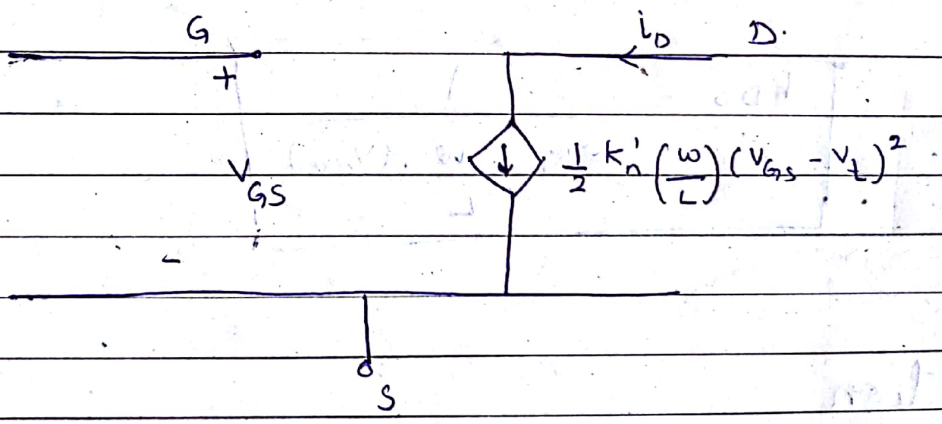
$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

Here i_D is independent of V_{DS}



it behaves as ideal current source.

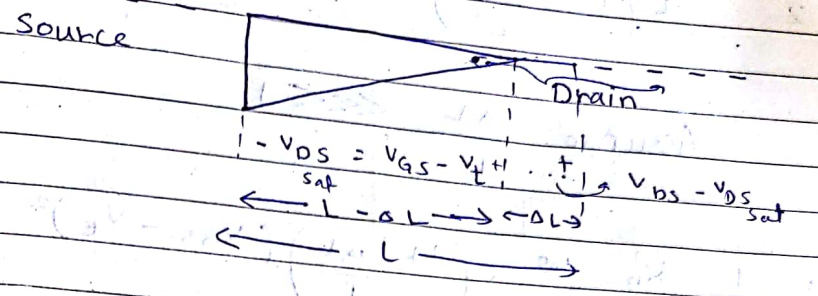
Large signal equivalent circuit model



At boundary $(V_{DS} = V_{GS} - V_t)$

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{DS})^2$$

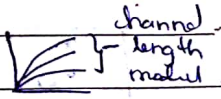
② Finite output resistance in saturation :-



Initially, a saturated mosfet is assumed to have ∞ resistance.

But in reality, as V_{DS} ↑, the pinch-off region shifts towards source, & due to V_{DS} ↑ the e^- in pinch-off region get attracted & move towards Drain, so there is some slight increase in drain current I_D even after saturation. This effect is channel length modulation

V_{DS} ↑ L ↓ i_D ↑ (small change



So, w.k.t $$i_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \quad \text{—— ①}$$

in satur, $L = L - \Delta L$

$$i_D = \frac{1}{2} K_n' \frac{W}{L - \Delta L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} K_n' \frac{W}{L\left(1 - \frac{\Delta L}{L}\right)} \times \left(1 + \frac{\Delta L}{L}\right)(V_{GS} - V_t)^2$$

$$\left(1 + \frac{\Delta L}{L}\right)$$

$$= \frac{1}{2} K_n' \frac{W}{L\left(1 - \frac{(\Delta L)^2}{L^2}\right)} \left(\frac{L + \Delta L}{L}\right) (V_{GS} - V_t)^2$$

Assume $\frac{\Delta L}{L} \ll 1$

$$i_D = \frac{1}{2} K_n' \frac{W}{L} \times \left(1 + \frac{\Delta L}{L}\right) (V_{GS} - V_t)^2 \quad \text{——(3)}$$

But $V_{DS} \propto \Delta L$

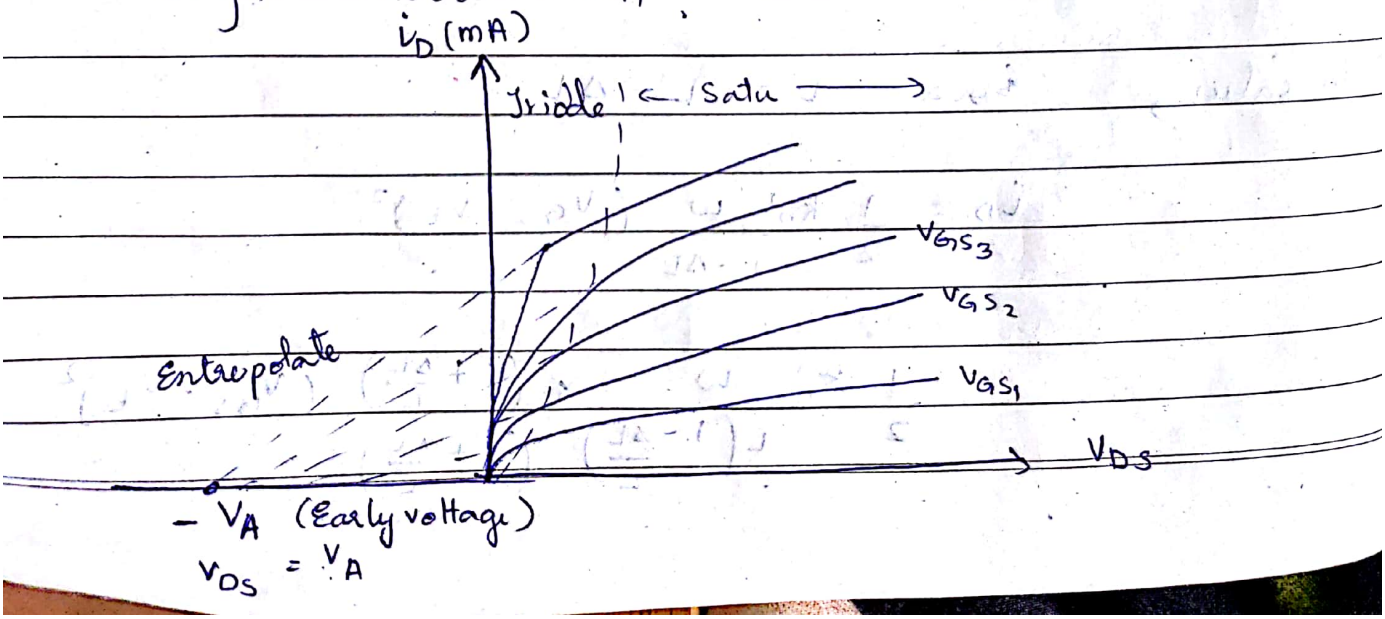
$\lambda' V_{DS} = \Delta L$

$$i_D = \frac{1}{2} K_n' \frac{W}{L} \left(1 + \frac{\lambda' V_{DS}}{L}\right) (V_{GS} - V_t)^2 \quad \text{——(4)}$$

Let $\lambda = \frac{\lambda'}{L} \Rightarrow \lambda' = \lambda L$

$$\boxed{i_D = \frac{1}{2} K_n' \frac{W}{L} (1 + \lambda V_{DS})(V_{GS} - V_t)^2}$$

current i_D when considered in channel length modulation.



from eq. if we substitute $v_{DS} = \frac{-1}{\lambda}$

i_D becomes '0'

So from graph $\boxed{v_A = \frac{1}{\lambda}}$

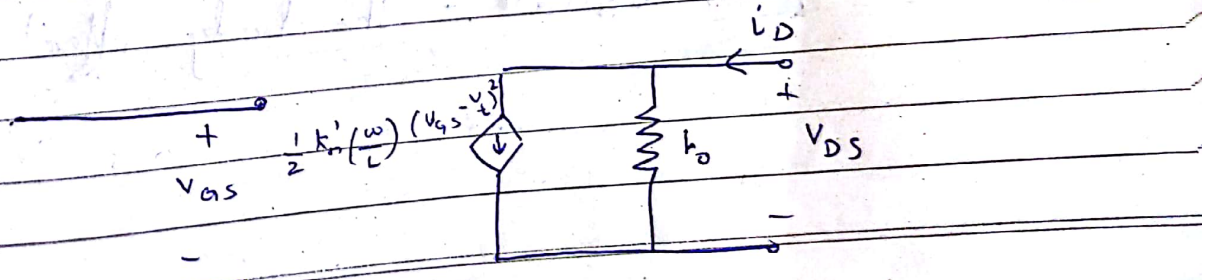
$$r_o = \left[\frac{i_D}{v_{DS}}\right]^{-1}_{v_{GS}} \quad \text{---} \quad (2)$$

$$r_o = \left[\frac{\frac{k_n'}{2}\left(\frac{w}{L}\right)(v_{GS} - v_t)^2(1+\lambda v_{DS})}{v_{DS}}\right]^{-1}$$

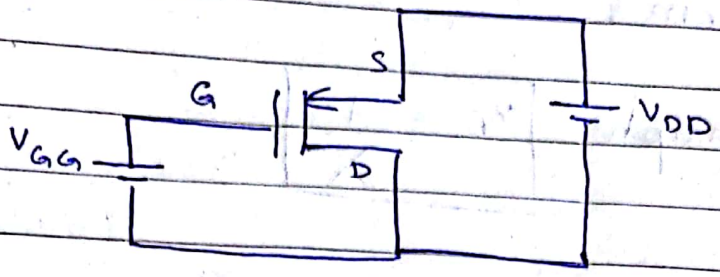
$$r_o = \left[\frac{\frac{k_n'}{2}\left(\frac{w}{L}\right)(v_{GS} - v_t)^2 \lambda v_{DS}}{v_{DS}}\right]^{-1}$$

$$r_o = \frac{1}{\lambda\left[\frac{k_n'}{2}\left(\frac{w}{L}\right)(v_{GS} - v_t)^2\right]}$$

$$r_o = \frac{1}{\lambda I_D}$$



Characteristics of the p-channel MOSFET



Since v_{GS} is -ve

$V_{GS} \leq V_t$

Triode :

$$V_{DS} > (V_{GS} - V_t)$$

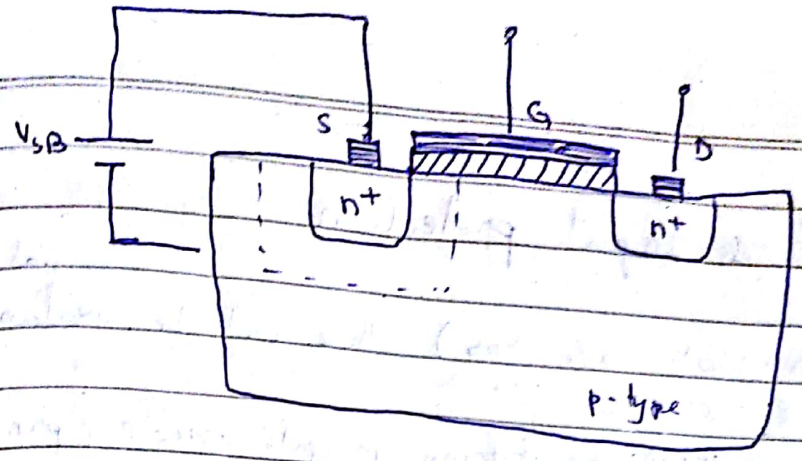
$$i_D = k_p' \left(\frac{W}{L}\right) \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$k_p' = \mu_p C_{ox}$ μ_p - mobility of holes.

Saturation $V_{DS} \leq (V_{GS} - V_t)$

$$i_D = \frac{k_p'}{2} \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

The role of substrate - The body effect



$$V_t = V_{to} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]$$

If voltage is applied to body, what is effect?

→ If Body & source a potential is applied, the e^- in source get attracted to +ve potential as body is at -ve potential, so channel depth decreases & $i_D \downarrow$.
So if we want channel back, we should increase $V_{GS} \uparrow$.

V_{to} - when 0 voltage b/n source & body

Temperature effects :-

* V_t → when $V_t \downarrow$ by 2mV for every 1° rise in temp, $i_D \uparrow$ ($i_D \propto V_{GS} - V_t$).

* k' → with increase in temp, $k' \downarrow$, so $i_D \downarrow$
$i_D \propto k'$
↓
This effect is more compared to V_t

So overall parameter, with $\downarrow k'$, i_D will $\downarrow$.

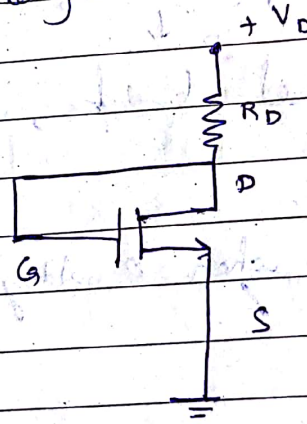
Breakdown & Input protection.

* V_{DS} (20V - 150V b/n V_{DS}) there will be avalanche breakdown (at p&n sub.)

* V_{GS} (above 30V) breakdown in gate oxide (permanent damage)

MOSFET circuits at DC

?] Design the following circuit to obtain a drain current of 80μA & also determine the DC voltage at the drain denoted as V_D. The NMOS transistor has $\mu_n C_{ox} = 200.\mu A/V$, $V_t = 0.6V$, $L = 0.8\mu m$, $W = 4\mu m$, Assume that there is no channel length modulation



→ Gate & Drain are shorted, it is diode connected MOS.

So $V_{DS} = V_{GS}$

for in saturation $V_{DS} \geq (V_{GS} - V_t)$ always in saturation

$$i_D = \frac{k'_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$80m\ i_{DD} = \frac{200\ H}{2}\left(\frac{4}{6.8}\right)(V_{GS} - (0.6)^2)$

$80\ mA = 100\ H\ (5)\ (V_{GS} - 0.36)$

$\frac{80 \times 10^{-3} \times 10^{6}}{100 \times 5} = V_{GS} - 0.36$

$160 + 0.36 = V_{GS}$

$\boxed{V_{GS} = 1.60 \times 36\ V}$

$R_D = \frac{V_{DS}}{i_D} = \frac{1}{80\mu} = 12.5\ k\Omega$ //

$V_{DS} = V_D - V_S = 1 - 0 = 1V$

$\boxed{V_D = 1V}$

$V_D = V_{DD} - I_D R_D$

$R_D = \frac{V_{DD} - V_D}{I_D} = 25k\Omega$ //

② Redesign the ckt of ex 1 to double the drain current I_D without changing V_D. Determine the new values of R_D & W/L ratio.

→

$\therefore I_D' = 160\mu A$

$V_D = 1V,$

$R_D = \frac{V_{DD} - V_D}{I_D'} = \frac{3 - 1}{} = 12.5k\Omega$ //

To find W/L

$$i_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

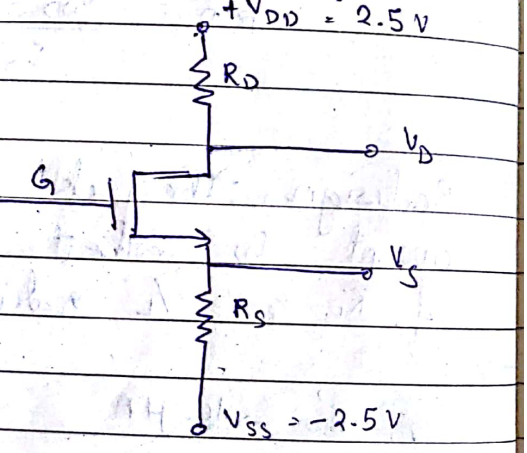
$$160\mu = \frac{200\mu}{2}\left(\frac{W}{L}\right)(1 - 0.6)^2$$

$$\left(\frac{W}{L}\right) = \frac{160\mu}{100\mu} \times \frac{1}{(0.4)^2}$$

$$= \frac{8}{5} \times \frac{1}{0.16}$$

$$\left(\frac{W}{L}\right) = 10$$

② Design the following circuit so that the transistor operates at $i_D = 0.4\,mA$, $V_D = 0.5\,V$, $V_t = 0.7\,V$, $\mu_n C_{ox} = 100\,\mu A/V^2$, $L = 1\,\mu m$, $W = 32\,\mu m$. Neglect channel length modulation.



→

$$R_D = \frac{V_{DD} - V_D}{i_D}$$

$$= \frac{2.5 - 0.5}{0.4m}$$

$$\boxed{R_D = 5\,k\Omega}$$

$V_G = 0$, $V_D = 0.5$ $\quad V_D > V_G$ (Sat region)

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$0.4\,m = \frac{1}{2} 100\,\mu \left(\frac{32}{1}\right)(V_{GS} - 0.7)^2$$

$$\frac{0.8\,m}{100\,\mu \times 32} = (V_{GS} - 0.7)^2$$

$$\frac{1}{2} + 0.7 = V_{GS}$$

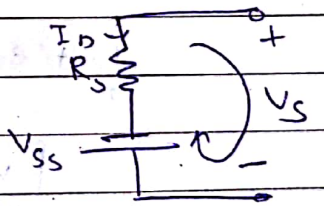
$$\boxed{V_{GS} = 1.2\,V}$$

$$V_{GS} = V_G - V_S$$

$$1.2 = 0 - V_S$$

$$\boxed{V_S = -1.2\,V}$$

Apply KVL near R_S



$$V_S + I_D R_S + 2.5 = 0$$

$$R_S = \frac{V_S + 2.5}{I_D}$$

$$= \frac{-1.2 + 2.5}{0.4\,m}$$

$$= 3.25\ K\Omega$$

4) Redesign the ckt of ex.3 when $V_{DD} = -V_{SS} = 2.5$
$V_t = 1V$, $\mu_n C_{ox} = 60 \mu A/V^2$, $(W/L) = 120\mu m/3\mu m$,
$I_D = 0.3mA$, $V_D = +0.4V$

→ $R_D' = ?$ $R_S' = ?$

$$R_D' = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.4}{0.3m} = 7k\Omega$$

$$R_S' = \frac{V_{SS} + V_S}{I_D} = \frac{+2.5 - 1.5}{0.3m} = 3.3k\Omega$$

$$I_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$0.3m = \frac{60\mu}{2}\left(\frac{120}{3}\right)(V_{GS} - 1)^2$$

$$\frac{0.3m}{30\mu \times 40} = (V_{GS} - 1)^2$$

$$\frac{1}{2} + 1 = V_{GS}$$

$$\boxed{V_{GS} = 1.5V}$$

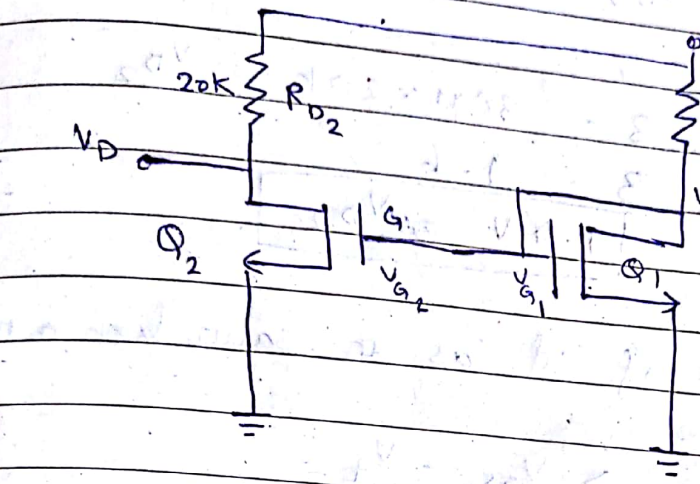
$$V_{GS} = V_G - V_S$$

$$\boxed{V_{GS} = -V_S = -1.5V}$$

(5) Consider the following ckt in which the MOSFET Q_1 has been already designed in Ex 1. Let the voltage of Q_1 is applied as gate voltage V_G. for the second mosfet Q_2, Assume that Q_2 is identical to Q_1. Find the i_D & V_D of Q_2.

($\frac{W}{L}$) & k_n' are same

→



From fig, $V_{G2} = V_{G1} = V_{D1} = 1V$

$$V_{GS_2} = V_{G2} - V_{S2}$$
$$= 1 - 0$$
$$\boxed{V_{GS_2} = 1V}$$

We assume the Q_2 is in saturation & find I_D in saturation

$$i_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$i_D = \frac{200\mu}{2}(5)(1 - 0.6)^2$$

$$= 100\mu\,(5)\,(0.4)^2$$

$$= 500\,\mu\,(0.16)$$

$$\boxed{I_{D_2} = 80\,\mu A}$$

$$V_{DD} - I_{D_2} R_{D_2} + V_{D_2} = 0$$

$$\frac{V_{DD} - V_{D_2}}{20k} = I_1$$

$$V_{DD} - I_{D_2} R_{D_2} = V_{D_2}$$

$$3 - 80\mu \times 20k = V_{D_2}$$

$$3 - 1.6$$

$$\boxed{1.4\,V = V_{D_2}}$$

Now crosscheck if it is in saturation or no.

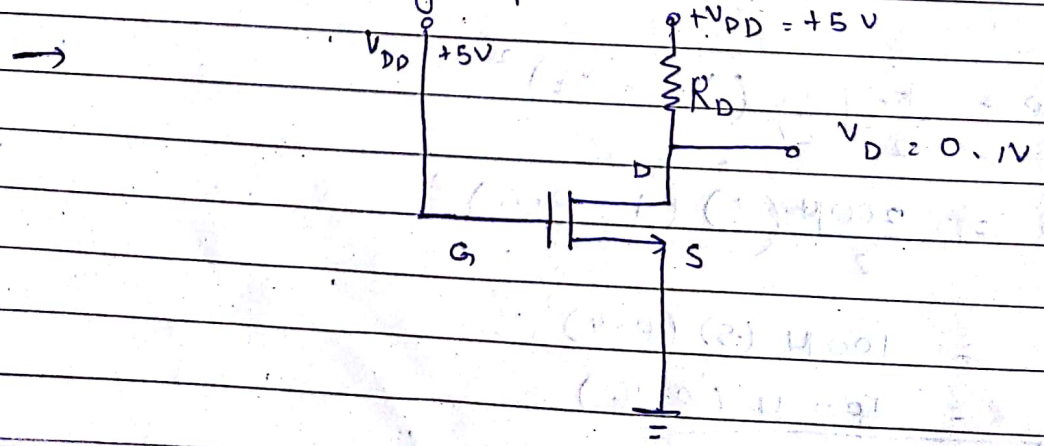
i.e $V_{DS_2} > V_{GS_2} - V_t$

$V_{D_2} - V_{S_2} > 1 - 0.6$

$1.4 > 0.4$

⑥ Design following ckt to establish drain voltage V_D of 0.1V given that $V_t = 1V$ & $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$.

Also find effective resistance b/n drain & source at this operating point.



$V_{DS} < V_{GS} - V_t$

$0.1 < 5 - 1$

$0.1 < 4$ Triode

So i_D in triode

$$i_D = k_n \left(\frac{W}{L}\right) \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$= 1m \left[(5-1)0.1 - \frac{0.01}{2}\right]$$

$$= 1m \ (0.4 - 0.005)$$

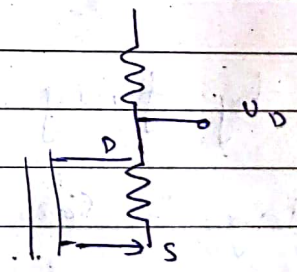
$$= 1m \ (0.395)$$

$$= 0.395 \text{ m A} \ //$$

$$R_D = \frac{V_{DD} - V_D}{i_D} = \frac{5 - 0.1}{0.395m} = 12.4 k\Omega$$

The effective resistance,

In triode region, it acts as linear resistance



So. $R_{eff} = \frac{V_D - V_S}{I_D} = \frac{0.1 - 0}{0.395m} = 253 \Omega$ //

⑦ In the circuit of previous problem if the value of R_D is doubled find approx value I_D & V_D.

→ $R_D' = 24.8\ K\Omega$

$$I_D' = \frac{I_D}{2} = 0.137\ mA \text{ //}$$

$$V_D' = V_{DD} - I_D' R_D'$$
$$= 0.1\ V \text{ //}$$

Biasing in MOS amplifier.

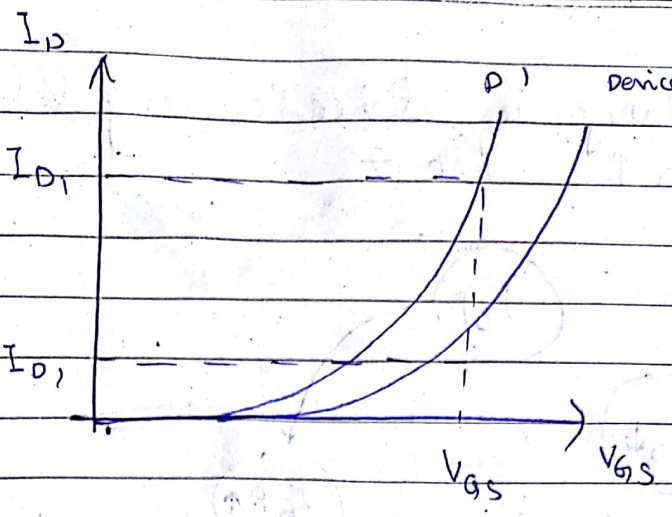
(1) By fixing V_{GS}
(2) By fixing V_{GS} and connecting source resistor R_S at source terminal.
(3) Connecting feedback resistor b/o gate & drain.
(4) Using constant current source.

(1) Biasing by fixing V_{GS}

→ ① Disadvantage : $C_{ox}, V_t, \frac{W}{L}$ will change if there is change in MOSFET.

In this biasing we fix V_{GS} so that I_D is fixed. if I_D fixed indirectly V_{DS} is fixed.

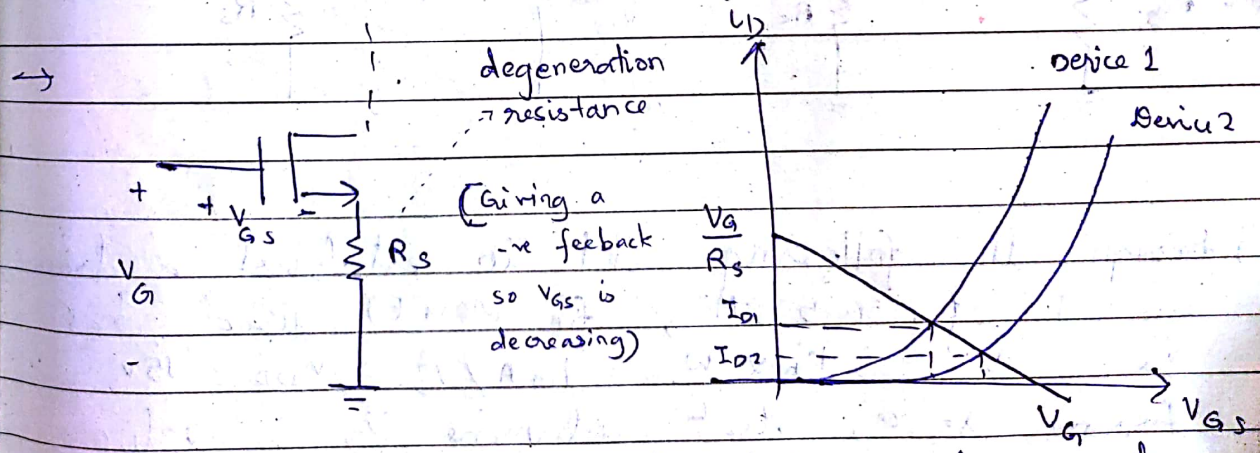
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$



NOTE ② For MOSFET to act as amplifier, it must be in saturation region, but using this biasing technique, it may or may not be in saturation region.

③ μ_n, V_t are temperature dependent if they change I_D will change

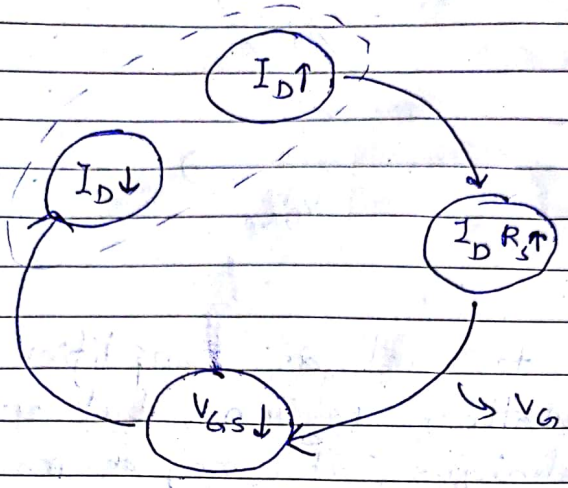
② Biasing by fixing V_G & connecting R_S at the source terminal.



We fix V_G & connect ent resistance at source terminal.

So, $V_G = V_{GS} + I_D R_S$

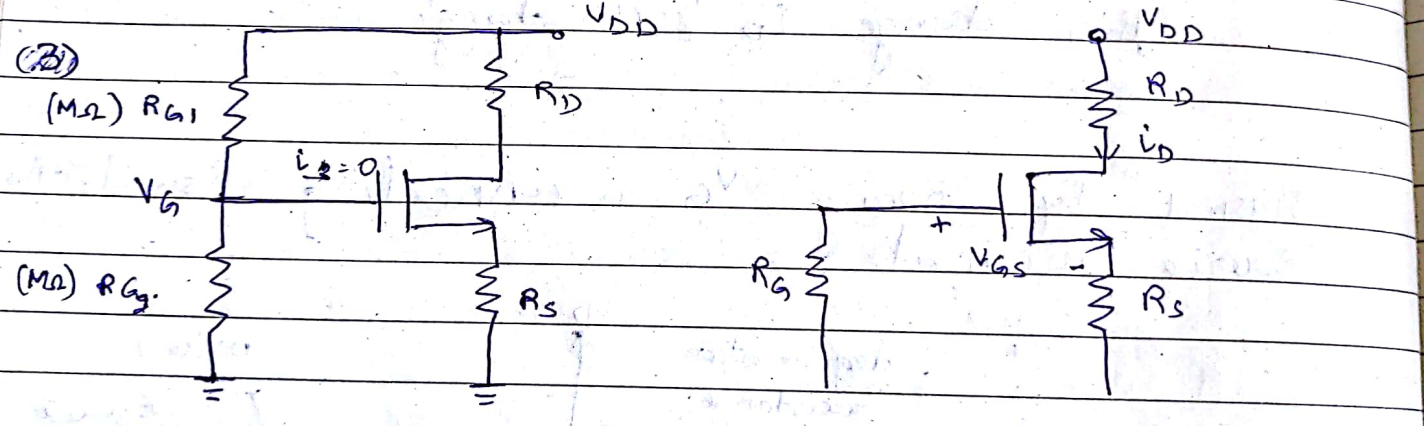
Now by change in device or any other parameter if $I_D \uparrow$ then —



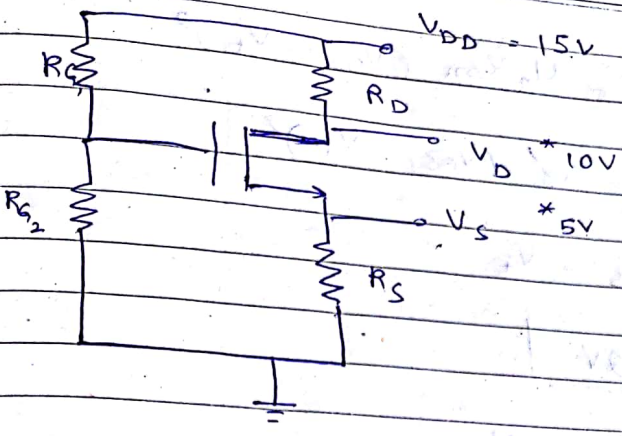
$\hookrightarrow V_G = V_{GS}\downarrow + I_D R_S\uparrow$

$\downarrow I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS}\downarrow - V_t)$

Circuit



?] Design the following ckt to establish a drain current of 0.5 mA, for MOSFET used has $V_t = 1V$, $k'_n \times \frac{W}{L} = 1mA/V^2$, $V_{DD} = 15V$, Assume $\lambda = 0$, Also determine % in value of I_D when MOSFET is resplaced by another MOSFET having same $k'_n \frac{W}{L}$ but $V_t = 1.5V$



→ When nothing is given we assume.

* Always $\frac{1}{3}^{rd}$ of V_{DD} is dropped across R_S.

remaining is V_D.

$\therefore V_D = 10V$

$V_S = 5V$

$V_{DS} = V_D - V_S$

$= 10 - 5$

$= 5V$

Using voltage divide

$$V_G = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}}$$

So to find V_G using sat. region fanula.

$$i_D = \frac{1}{2} k_n' \mu_n C_{ox} (V_{GS} - V_t)^2$$

$$0.5m = \frac{1}{2} \times 1m (V_{GS} - V_t)^2$$

$$1 = V_{GS} - V_t$$

$$\boxed{V_{GS} = 2V}$$

$$V_{GS} = V_G - V_S$$

$$2 = V_G - 5$$

$$\boxed{V_G = 7V} \longrightarrow (2)$$

$$V_G = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}}$$

$$7 = \frac{15\, R_{G2}}{R_{G1} + R_{G2}}$$

$$7R_{G1} + 7R_{G2} = 15R_{G2}$$

$$\boxed{7R_{G1} = 8R_{G2}}$$

R_{G1} & R_{G2} are equal only when $R_{G1} = 8M\Omega$ & $R_{G2} = 7M\Omega$

$$V_{DD} - R_D I_D = 0$$

$$R_D = \frac{V_{DD}}{I_D}$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = 10K\Omega \;//$$

$$R_S = \frac{V_S}{I_D} = 10\,k\Omega$$

(ii) If $V_t = 1.5\,V$.

$V_{GS} = ?$ $\quad V_{GS} = V_G - V_S$

$\quad = V_G - I_D R_S$

$\boxed{V_{GS} = 7 - 10 I_D}$

~~V_{GS} is same.~~

$$i_D = \frac{1}{2} K_n' C_{ox} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} \cdot 1m \cdot (2 - 1.5)^2$$

$$\boxed{i_D = 0.125\,mA}$$

$$i_D = \frac{1}{2} K_n' C_{ox} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} K_n' C_{ox} ((7 - 10 I_D) - 1.5)^2$$

$$i_D = \frac{1}{2} K_n C_{ox} (5.5 - 10 I_D)^2$$

$$2 i_D = 1m (30.25 + 100 I_D^2 - 110 I_D)$$

$$2K i_D = 30.25 - 100 i_D^2 + 110 i_D$$

$$2.1K i_D - 110 i_D = 30.25$$

$$2100 i_D - 110 i_D^2 = 30.25$$

$$110 i_D^2 - 2100 i_D + 30.25 = 0$$

$I_D = 0.6665\,mA$ $\quad I_D = 0.45\,mA$

$V_t = 1V$ $\quad I_D = 0.5\,mA$

$\boxed{V_t = 1.5\,V \quad I_D = 0.45\,mA}$

So $I_D < 0.5$

% change in I_D $= \frac{I_{D_2} - I_{D_1}}{I_{D_1}}$

$= 0.45m - 0.50m \,/0.5$

$= -0.05m$

$\therefore$ 10% decrease

9.2%

?] Repeat previous problem when fixed V_{GS} is used then find the req. value of V_{GS} to get a DC biased current i_D of 0.5 mA but with first device parameters as $V_t = 1V$, $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$.

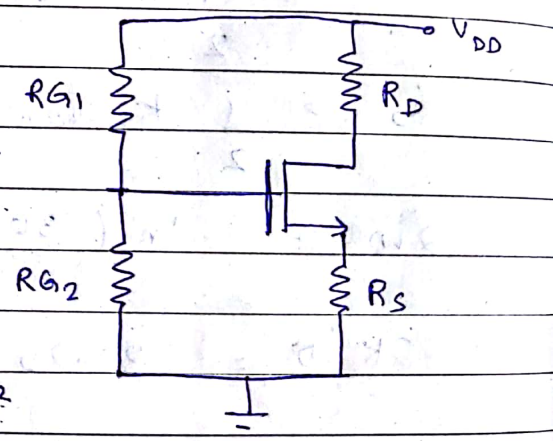
also determine % change in i_D, when the first MOS is replaced by second one with V_t (1.5) V.

→ Find RG_1, RG_2, R_S, R_D

Thumb rule (Assume)

like previous.

$V_{GS_1} = 2V$



$V_t = 1.5V$ $\quad i_{D_2} = \frac{1}{2} Con\, K_n \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$

$= \frac{1}{2}(1)(4 - 1.5)^2$

$= \frac{1}{2} \times \frac{1}{4}$

$I_{D_2} = 0.125\,mA$

% change $= \frac{I_{D_2} - I_{D_1}}{I_{D_1}}$

$= \frac{0.125 - 0.50}{0.5}$

$= 75\%$ decrease

so this method biasing is also not efficient

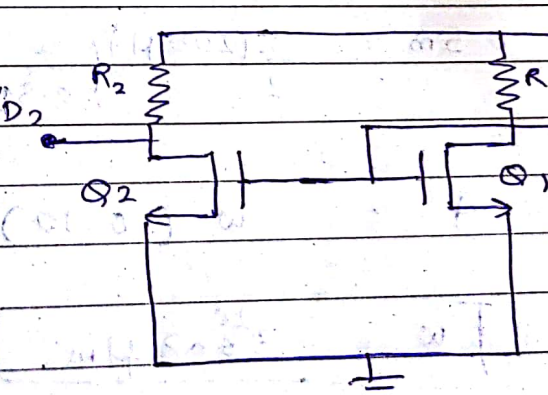
Problems on DC MOSFET

16/10/18

(8) Let Q_1 & Q_2 have $V_t = 0.6V$, $\mu_n C_{ox} = 200 \mu A/V^2$, $L_1 = L_2 = 0.8 \mu m$, $W_1 = 8 \mu m$ & the channel length modulation $\lambda = 0$.

(a) Find the value of R_1 to establish the current of 0.2 mA in Q_1.

(b) Find W_2 & new value of R_2 so that Q_2 operates in the saturation region with the current of 0.5 mA and drain voltage of 1V.



→ $V_t = 0.6V$

$\mu_n C_{ox} = 200 \mu A/V^2$.

Q_1 is diode connected MOSFET so $V_{GS} = V_{D_1}$

$V_S = 0$

$$i_{D_1} = \frac{1}{2} k'_n \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$0.2m = \left(\frac{0.8}{0.8}\right) 100 \mu (V_{GS} - 0.6)^2$$

$$\boxed{V_{GS} = 1.047 \text{ V}}$$

$$V_{GS_1} = V_{DS_1} = V_{D_1} - V_{S_1}$$

$$1.047 = V_{D_1} - 0$$

$$\boxed{V_{D_1} = 1.047\ V}$$

KVL,

$$R_1 = \frac{V_{DD} - V_{D_1}}{i_{D_1}}$$

$$= \frac{3 - 1.047}{0.2\ m}$$

$$\boxed{R_1 = 9.7\ K\Omega}$$

Case II: WKT assuming $V_{GS_1} = V_{GS_2}$ & it is in saturation

$$I_{D_2} = \frac{1}{2} k_n \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$0.5m = \frac{1}{2}(200\mu)\left(\frac{w}{0.8\mu}\right)(1.047 - 0.6)^2$$

$$4 = w\ (0.12)$$

$$\boxed{w = \frac{20}{3}\ \mu m}$$

$$R_2 = \frac{V_{DD} - V_{D_2}}{I_{D_2}} = 4k2$$

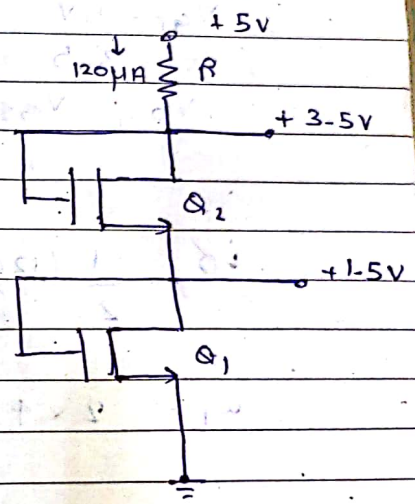
7] The N-mos transistor used in following circuit is having $V_t = 1V$, $\mu_n C_{ox} = 120 \mu A/V^2$.

$\mu_n C_{ox} = 120 \mu A/V^2$

$\lambda = 0$,

$l_1 = l_2 = 1 \mu m$. (w_1 & w_2).

Find the required values of gate widths for each of Q_1 & Q_2 when the value of R to obtain the voltage & current values as indicated in figure.



→ $w_1 = ?$

$w_2 = ?$

From fig ① $V_{D_1} = 1.5V = V_{GS_1}$

$i_D = \frac{1}{2}(120\mu)\left(\frac{w_1}{1}\right)(1.5 - 1)$

$2 \times 120\mu = 120\mu (w_1)(0.5)^2$

$\boxed{w_1 = 8 \mu m}$

② Now find w_2

wk $V_{G_2} = V_{D_2} = 3.5V$

$V_{S_2} = 1.5V$ (from fig)

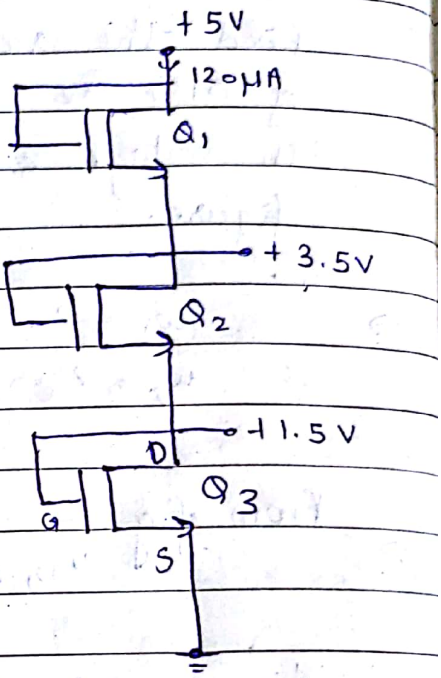
$V_{GS_2} = V_{D_2} - V_{S_2} = \boxed{2V}$

$i_D = \frac{1}{2}(120\mu)\left(\frac{w_2}{1}\right)(2 - 1)^2$ ③ $R = \frac{V_{DD} - V_{D_2}}{i_{D_2}(H)}$

$\boxed{w_2 = 2 \mu m}$

$\boxed{R = 12.5 k\Omega}$

(10) The NMOS transistors used in following ckt have $V_t = 1V$, $\mu_n C_{ox} = 120 \mu A/V^2$, $\lambda = 0$, $L_1 = L_2 = L_3 = 1 \mu m$. Find the eq. values of gate width for each of the transistors to obtain V & I values as indicated in fig.



→ $w_1 = ?$

$V_{G_1} = 5V$

$V_{S_1} = 3.5$

$V_{DS_1} = V_{GS_1} = 5 - 3.5$

$= 1.5V$

$$i_D = \frac{1}{2}(120\mu)\left(\frac{w_1}{1\mu}\right)(1.5-1)^2$$

$$w_1 = 2 \times 4 = 8 \mu m$$

$w_2 = .2 \mu m$ (previous swim)

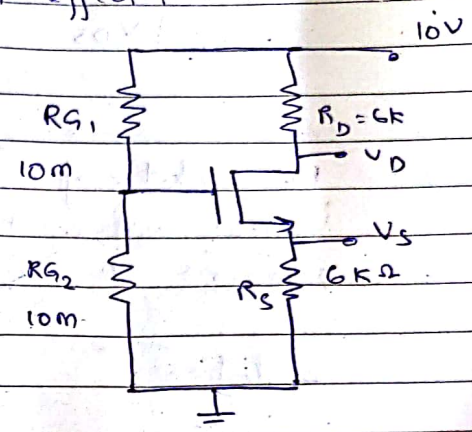
$w_3 = ?$

$V_{D_3} = 1.5V = V_{GS_3}$

$$i_D = \frac{1}{2}(120\mu)\left(\frac{w_3}{1}\right)(1.5-1)^2$$

$$\boxed{w_3 = 8 \mu m}$$

(12) Analyze the following ckt to determine the voltages at all nodes & the current through all branches given that $V_t = 1V$, $k'_n\left(\frac{W}{L}\right) = 1\ mA/V^2$. Neglect the channel length modulation effect.



→ I_D, V_D, V_S, V_G ?

$$V_G = \frac{10 \times R_{G2}}{R_{G1} + R_{G2}}$$

$$= 5V$$

V_S = ?

$$V_{GS} = V_G - V_S$$

$$V_{GS} = 5 - 6K I_D$$

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$i_D = \frac{1}{2}(1)\left[5 - 6K I_D - 1\right]^2$$

$$2 i_D = (5 - 1 - 6K I_D)^2$$

$$\sqrt{2 i_D} = 4 - 6K I_D$$

$\boxed{i_D = 0.88\ mA}$ $\qquad$ $\boxed{i_D = 0.5\ mA}$

$V_{GS} = 5 - 6 I_D$

$= -0.34V$ //

$V_{GS} = 5 - 3$

$= 2V$ //

$V_S = 6 I_D = \boxed{3V}$

~~$V_{DS} = V_D - V_S = 10$~~

$$V_D = 10 - 6 I_D - 3$$

$$= 6.0.7$$

$$\therefore \boxed{V_{DS} = 4V}$$

Q 11) For ckt of previous example what is the largest value rd can have while transistor remains in saturation mode.

Condition $V_{DS} \geq V_{GS} - V_t$

$$V_{DS\,min} = V_{GS} - V_t$$

$$V_{D\,min} - V_S = V_G - V_S - V_t$$

$$V_{D\,min} = V_G - V_t$$

$$= 5 - 1$$

$$= 4V //$$

$$R_{D\,max} = \frac{V_{DD} - V_{D\,min}}{i_D}$$

$$= \frac{10 - 4}{0.5}$$

$$= 12 k\Omega //$$

? Redesign the ckt of previous example for following requirements -

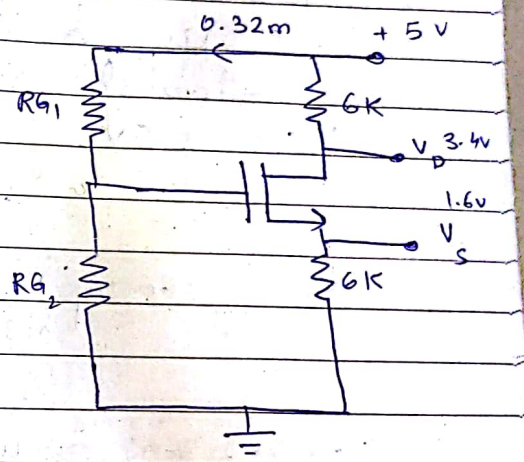
$V_{DD} = +5V$

$i_D = 0.32\ mA$

$V_S = 1.6V$

$V_D = 3.4V$

with a 1 μA current through the voltage divider R_{G_1}, R_{G_2}, assume the same MOSFET, with $V_t = 1V$, $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$, $\lambda = 0$.



→ $V_G = ?$

$$i_D = \frac{1}{2}(1m)(V_G - 1.6 - 1)^2$$

$$\sqrt{0.64} = V_G - 2.6$$

$$V_G = 3.4\ V$$

$$V_{GS} = 3.4 - 1.6$$

$$= 1.8\ V //$$

$$V_G = \frac{V_{DD} \cdot R_{G_2}}{R_{G_1} + R_{G_2}}$$

$$1.8 = \frac{5 R_{G_2}}{R_{G_1} + R_{G_2}}$$

$$3.4 R_{G_1} = 1.6 R_{G_2}$$

$R_{G_1} = 1.6\ M\Omega$

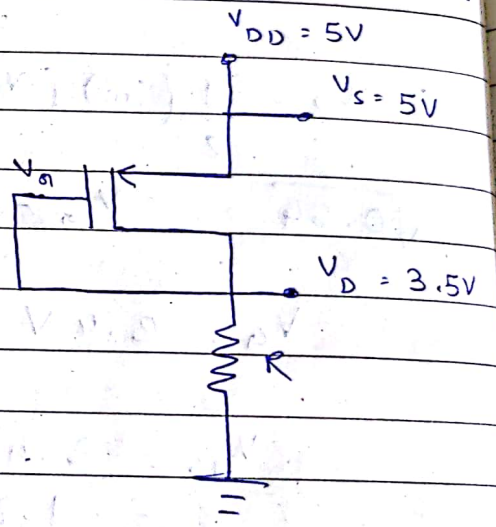
$R_{G_2} = 3.4\ M\Omega$

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= 5\,k\Omega$$

$$R_S = \frac{V_S}{I_D} = 5\,k\Omega$$

2] PMOS shown has $V_t = -0.7V$, $\mu_p C_{ox} = 60\,\mu A/V^2$, $l = 0.8\,\mu m$ & $\lambda = 0$. Determine w & R in order to establish drain current of 115 μA & $V_D = 3.5V$.



→

$$i_D = \frac{1}{2}(60\mu)\left(\frac{w}{0.8}\right)(-1.5+0.7)^2$$

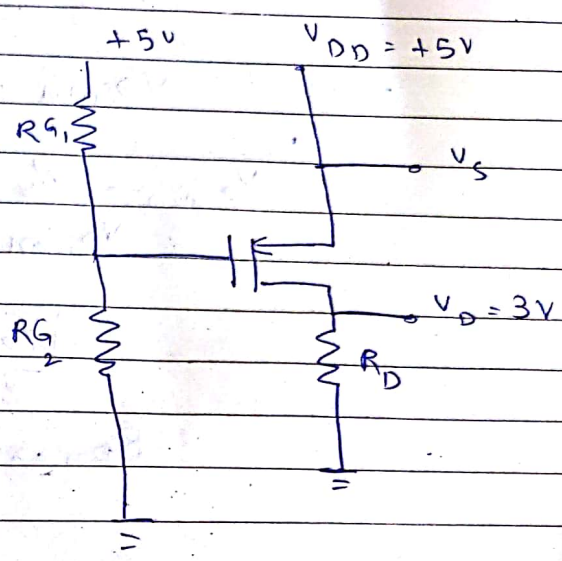
$$\frac{115 \times 2 \times 0.8}{60 \times (4\text{8}4)(0.64)} = w$$

$$\boxed{w = 5.5\,\mu m}$$

0.736 μm // 1.96 μm // And (4.79 μm) ✓

$$R = \frac{V_D}{i_D} = \frac{3.5}{115\mu} = 30.4\,K\Omega$$ //

2] Design following enchanment type PMOS ckt operated in saturation with $i_D = 0.5\,mA$, $V_D = +3\,V$, $V_t = -1V$, $K_p'\left(\frac{W}{L}\right) = 1mA/V^2$



→ Ans:

$V_{GS} = -2V$

$V_G = 3V$

$RG_1 = 2M\Omega$

$RG_2 = 3M\Omega$

$R_D = 6k\Omega$

$$i_D = \frac{1}{2}(1m)(V_{GS} + 1)^2$$

$$\pm 1\,m = \frac{1}{2}(1m)(V_{GS} + 1)^2$$

For PMOS you should take - negative

$$V_{GS} = -2V$$

$$V_S = 5V$$

$$V_{GS} = V_G - V_S$$

$$-2 + 5 = V_G$$

$$V_G = 3V$$

$$RG_1 = \frac{5 - 3}{0.5m} = \frac{3 = 5 \times RG_2}{RG_1 + RG_2}$$

$$3RG_1 = 2RG_2$$

$$RG_1 = 2M\Omega$$

$$RG_2 = 3M\Omega$$

$$R_D = \frac{V_D}{i_D} = \frac{3}{0.5} = 6k\Omega$$

(b) What is largest value of R_D that will maintain pmos still in saturation

$$V_{DS} \leq V_{GS} - V_t$$

$$V_{DS\,max} = V_{GS} - V_t$$

$$V_{D\,min} - V_S = V_G - V_S - V_t$$

$$V_{D\,max} = V_G - V_t$$

$$= 3 + 1$$

$$\boxed{V_{D\,max} = 4V}$$

$$R_{D\,max} = \frac{V_{D\,max}}{i_D}$$

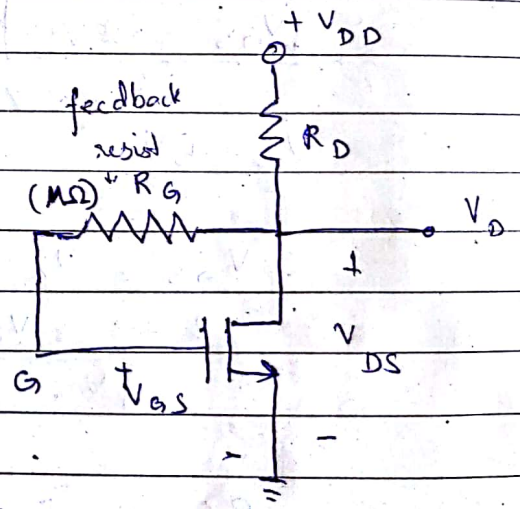
$$= 8K\Omega \text{ //}$$

3. Biasing using a drain-to-gate feedback resistor

→ $V_S = 0$, $V_D = V_G$

$$V_{DS} = V_{GS} = V_{DD} - I_D R_D$$

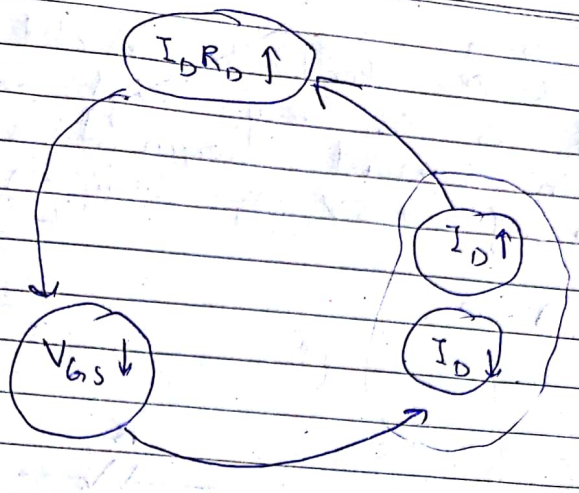
$$V_{DD} = V_{GS} + I_D R_D \quad \text{—①}$$



MOSFET is in sat^n.

$$I_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \quad \text{—②}$$

$\lambda = 0$



- We connected R_G to want high i/p impedance, since it is very high, potential at gate & source is same.

So $V_{DS} = V_{GS}$

Since it is diode connected mos, it is in satn.

$$V_{DD} = V_{GS} + I_D R_D$$

if $I_D \uparrow$, to compensate $V_{GS} \downarrow$

if $V_{GS} \downarrow$, " $I_D \downarrow$.

That is how will maintain Q. point in sat.

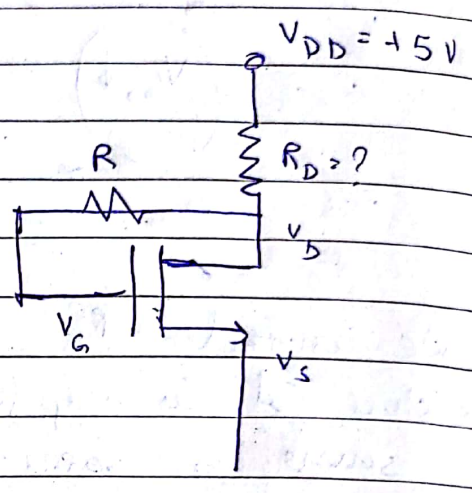
NOTE: In real, there is no use of R_G much, it can be shated.

If voltage source is applied, it can act as amplifier

D to G

3] Design gate-to-drain feedback resistor, resistance b/n D and G is very high resistance & the DC drain current required is of 0.5 mA. Assume V_{DD} of +5V & $k_n'\left(\frac{W}{L}\right) = 1mA/V^2$.

$V_t = 1V$ & $\lambda = 0$.



$\rightarrow I_D = 0.5m$

$$I_D = \frac{1}{2} k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$0.5m = \frac{1}{2}(1m)(V_{GS} - 1)^2$$

$$1 = V_{GS} - 1$$

$$\boxed{V_{GS} = 2V} = V_{DS} = V_D$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = 6k\Omega = \frac{5-2}{0.5m}$$

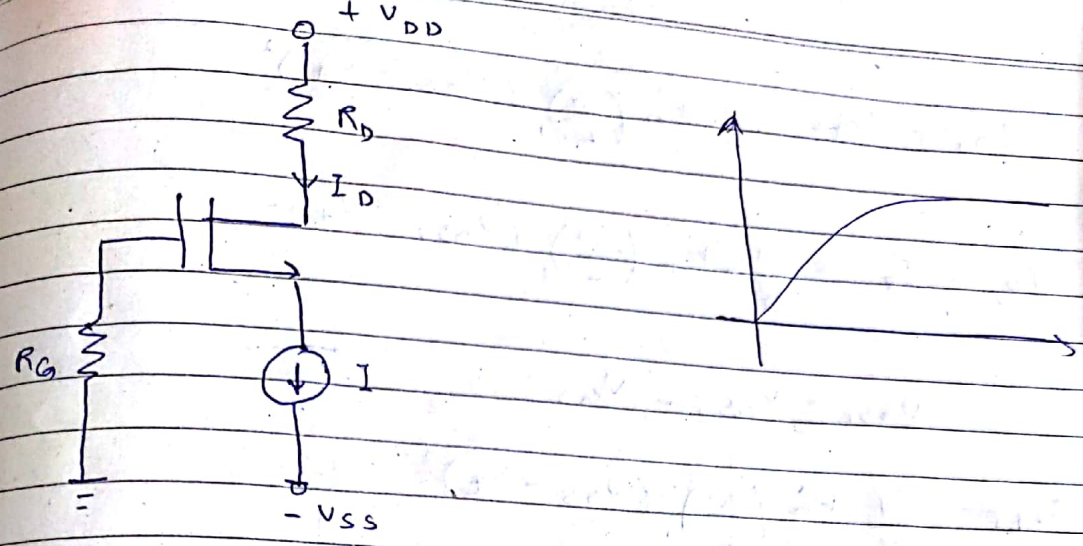
(4. Biasing using a constant current source.

Biasing a const current source at source terminal, here also a large value of R_G is used, so that it offers a high resistance to signal connected to gate.

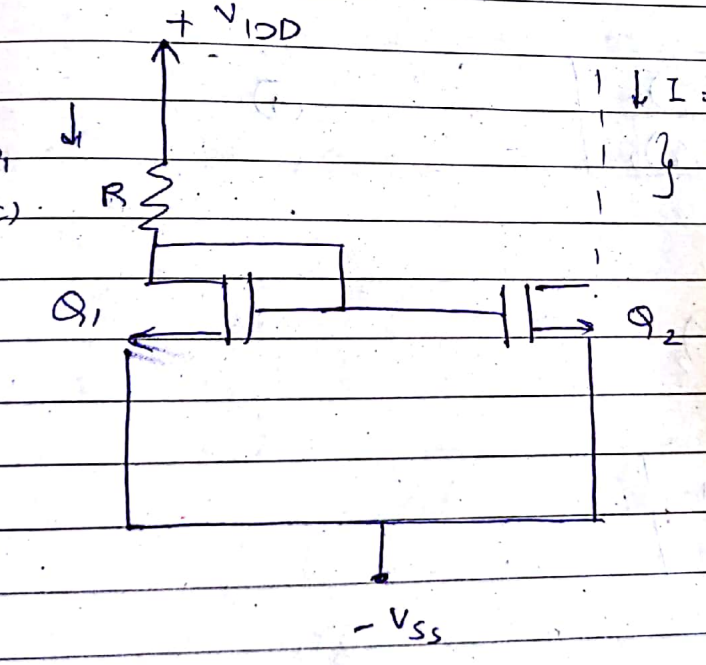
Value of R_D will decide V_D.

value of V_D will decide if signal is distorted

So by fixing I, $I = I_S = I_D$.



Current mirror : ckt to generate that const current



$I = I_{D_2}$

} we connect a resistance here such that Q_2 in satn.

Assume $k_n \left(\frac{W}{L}\right)$, V_t = Q_1 & Q_2 are equal.

Case 1: $\left(\frac{W}{L}\right)_1 \neq \left(\frac{W}{L}\right)_2$

$$I_{D_1} = I_{REF} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS_1} - V_t)^2$$

$$I_{D_2} = I_o = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS_2} - V_t)^2$$

$$V_{GS_1} = V_{GS_2} = V_{GS}$$

$$I_{REF} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

$$I = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2$$

Current ratio

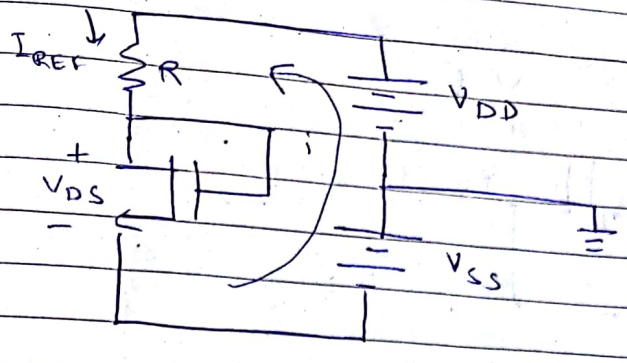
$$\boxed{\frac{I}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}} \quad \text{---------- (1)}$$

Case 2: $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$

$$\boxed{\frac{I}{I_{REF}} = 1}$$

- To find value of R in Q_1,

Consider Q_1



$$V_{DD} + V_{SS} - V_{DS} - I_{REF} R = 0 \quad \text{—— (1)}$$

$$V_{DS} = V_{GS}$$

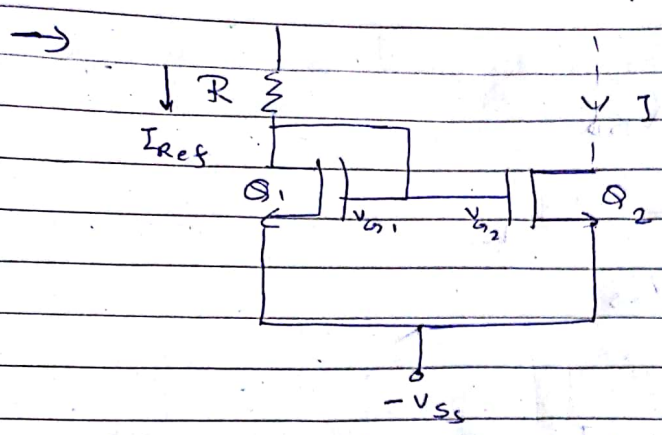
$$V_{DD} - I_{REF} R - V_{GS} + V_{SS} = 0$$

$$\boxed{R = \frac{V_{DD} - V_{GS} + V_{SS}}{I_{REF}}} \quad \text{—— (3)}$$

(?) In a current mirror ckt using transistors Q_1 & Q_2, the length of both channels are equal, but width are elevated by $\frac{W_2}{W_1} = 5$, design the ckt to obtain I of 0.5 mA, given that $V_{DD} = -V_{SS} = 5V$ & $K_n'\left(\frac{W}{L}\right)$, $= 0.8 mA/V^2$, $V_t = 1V$, $\lambda = 0$.

(a) What is the voltage at the gates of Q_1 & Q_2.

(b) What is the lowest voltage allowed at the drain of Q_2 so that Q_2 remains in sat^n.



$$\frac{I}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} = 5$$

$$I = 5 \times I_{REF}$$

$$0.5m = 5 \times 0.5m\, I_{Ref}$$

$$\boxed{I_{Ref} = 0.1\,m}$$

$$I_{Ref} = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$0.1m = \frac{1}{2} \times 0.8m (V_{GS} - 1)^2$$

$$\frac{1}{4} = V_{GS} - 1$$

$$V_{GS} = \frac{3}{2} V$$

$$\boxed{V_{GS} = 1.5\,V}$$

'-' sign of V_{GS} is already derived as -ve it self so take +ve.

$\therefore \quad V_{GS} = V_{DS} = V_D$

$$R = \frac{V_{DD} - V_{DS} + V_{SS}}{I_{REF}}$$

$$= \frac{5 - 1.5 + 5}{0.1\,m}$$

$$= 85\,k\Omega //$$

(ii) $V_{G1} = V_{G2}$

$V_{GS_1} = 1.5\,V$

$V_{G_1} - V_{S_1} = 1.5$

$V_{G_1} = 1.5 + V_{S_1}$ → Here -ve is not taken in account

$= 1.5 - 5$

$\boxed{V_{G1} = -3.5\,V}$

(iii) $V_{DS} \geq V_{GS} - V_t$ satn.

$V_{DS_{min}} = V_{GS} - V_t$

$= 1.5 - 1$

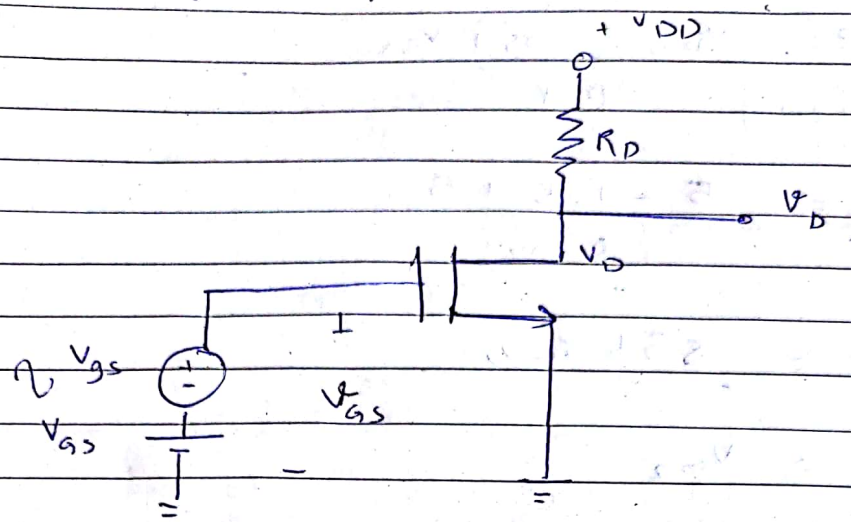
$V_{D_m} - V_{S_m} = 0.5$

$V_{D_m} = 0.5 - 5$

$\boxed{V_{D_{min}} = -4.5\,V}$

26.10.18

Small signal operation & models



Behaviour of MOSFET in small ac signal, for MOSFET to act as amplifier, it must be in saturation.

(i) DC bias point

Take $V_{gs} = 0$,

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$V_D = V_{DD} - I_D R_D$$

$$\boxed{V_D \geq V_{GS} - V_t}$$ for amplification.

(iii) The signal current in the drain terminal.

For v_{gs} with some dc voltage. → instantaneous value.

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \quad -①$$

$$v_{GS} = V_{GS} + v_{gs} \quad -②$$

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)((V_{GS} + v_{gs}) - V_t)^2$$

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(\underbrace{V_{GS} - V_t}_{a} + \underbrace{v_{gs}}_{b})^2$$

$$i_D = \underbrace{\frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)^2}_{DC} + k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n' \left(\frac{W}{L}\right) v_{gs}^2$$

v_{gs}^2 → non-linear distraction.
⇒ Harmonic term in signal

This value so be made small so that we can ignore it.

$$= \frac{1}{2} k_n' \left(\frac{W}{L}\right) v_{gs}^2 << k_n' \left(\frac{W}{L}\right)(V_G - V_t) v_{gs}$$

So, $$\frac{v_{gs}}{2} << V_{GS} - V_t$$

$$\boxed{v_{gs} << 2(V_{ov})}$$ overdrive

or

$$v_{gs} << 2(V_{GS} - V_t)$$

$$i_D = I_D + i_d \quad \text{——} \circledast$$

$$i_d = k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t) v_{gs}$$

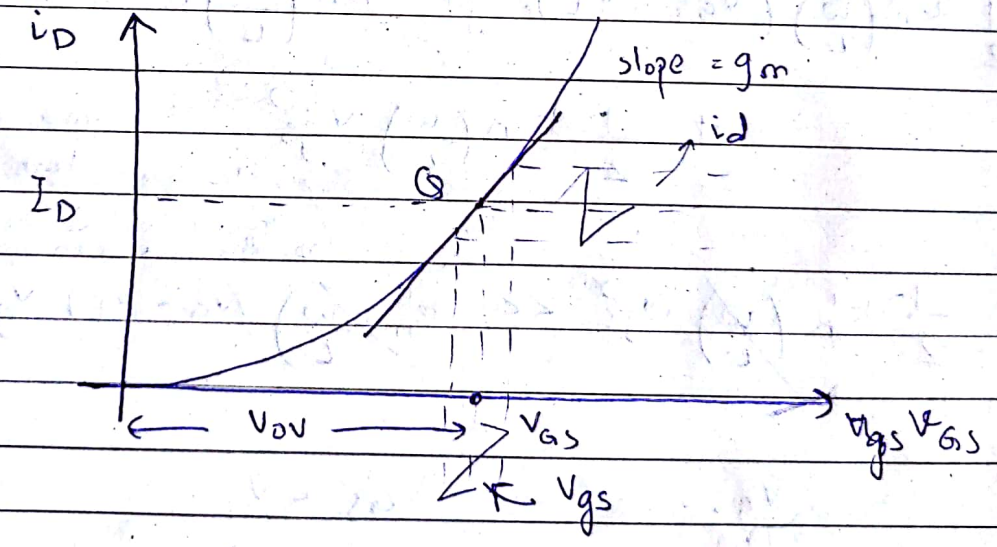
$$\frac{i_d}{v_{gs}} = k_n' \left(\frac{W}{L}\right) (V_{OV})$$

termed as

(g_m) → small signal transconductance.

$$\boxed{g_m = k_n' \left(\frac{W}{L}\right) (V_{OV})}$$

Graphical method. to find g_m.



$$\text{Slope} = \frac{\Delta x}{\Delta y} = g_m = \frac{i_d}{v_{gs}}$$

Voltage gain (A_v) [How much times it is amplified]

→ Ratio of o/p v by i/p v.

$$v_D = V_{DD} - i_D R_D \quad \text{—①}$$

$$i_D = I_D + i_d \quad \text{—②}$$

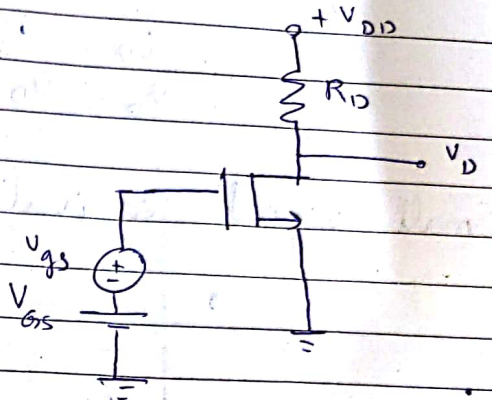
$$v_D = V_{DD} - (I_D + i_d) R_D$$

$$= V_{DD} - I_D R_D - i_d R_D \quad \text{—③}$$

$$v_D = \underbrace{V_D + v_d} \quad \text{—④}$$

sum of dc & due to ac source.

$$\boxed{v_d = -i_d R_D}$$



To get i/p voltage in picture.

$$g_m = \frac{i_d}{v_{gs}} \Rightarrow i_d = v_{gs} g_m \quad \text{—⑤}$$

$$\therefore \boxed{v_d = -v_{gs} g_m R_D}$$

$$A_v = \boxed{\frac{v_d}{v_{gs}} = -g_m R_D}$$

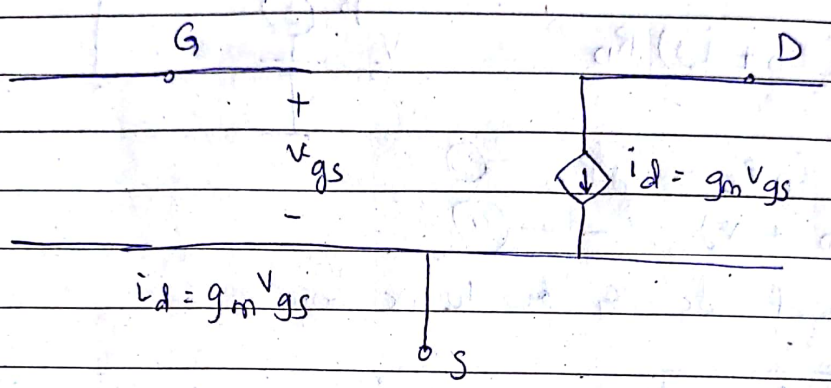
Seperating the DC analysis & the signal analysis.

- analyze the dc part & then add ac component.

$$i_D = I_D + i_d$$

$$v_D = V_D + v_d$$

Small signal equivalent models

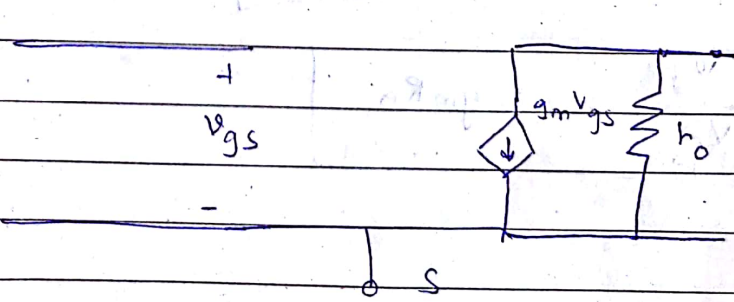


Here we can't consider channel length modulation

$$r_o = \frac{V_A}{I_D}$$

$$I_D = \frac{1}{2}\left(k_n' \frac{W}{L}\right)(V_{GS} - V_t)$$

$V_A = \frac{1}{\lambda}$ for some λ.



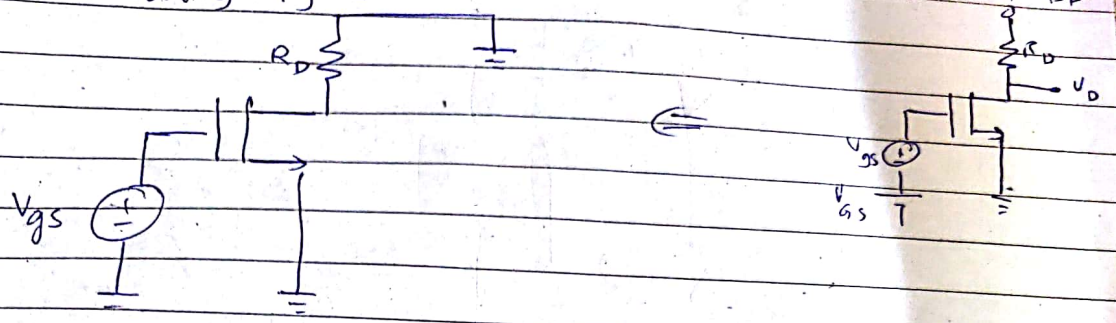
For if $\lambda = 0$

$V_A = \infty$ $\quad r_o = \frac{\partial}{I_D} = \infty$.

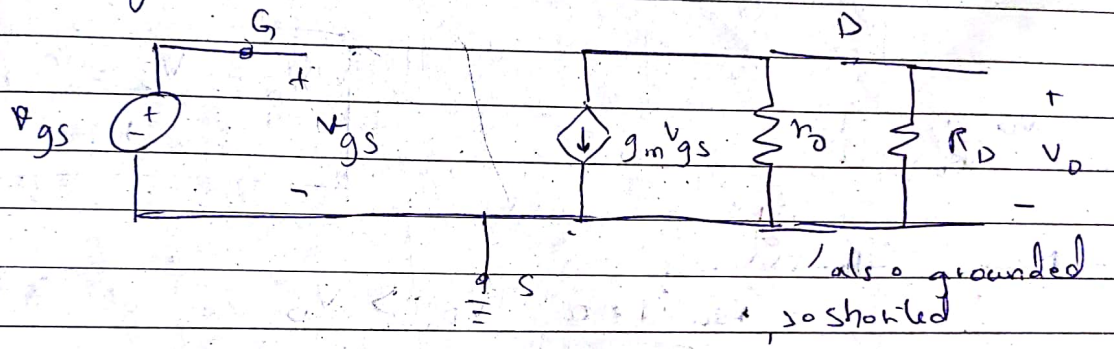
→ → →

AC equivalent for small signal.

Taking only ac



Small signal model :-



(if we ignore λ, no r_o)

$$A_V = \frac{V_o}{V_i} = \frac{V_{ds}}{V_{gs}} = \frac{-g_m(V_{gs})(r_o \| R_D)}{V_{gs}}$$

$$\boxed{A_V = -g_m(r_o \| R_D)}$$

Continued in maths book ....

After maths DC ...

26.10.18

Small signal transconductance.

$$g_m = k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)$$

$g_m \uparrow$ ← $\frac{W\uparrow}{L\downarrow}$, $V_{GS}\uparrow$

$\propto$

$\uparrow i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)$

$\downarrow V_D = V_{DD} - i_D R_D$

So we usually go for $\frac{W\uparrow}{L\downarrow}$

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \quad \text{— ①}$$

$$\rightarrow \quad k'_n \left(\frac{W}{L}\right) = \frac{2 i_D}{(V_{GS} - V_t)^2} \quad \text{— ②}$$

Substitute eq ② in eq ③

$$g_m = \frac{2 i_D}{(V_{GS} - V_t)^2}(V_{GS} - V_t)$$

$$\boxed{g_m = \frac{2 i_D}{V_{GS} - V_t}}$$

$$\Rightarrow \frac{2i_D}{k_n'\left(\frac{W}{L}\right)} = (V_{GS} - V_t)^2$$

$$\Rightarrow V_{GS} - V_t = \sqrt{\frac{2i_D}{k_n'\left(\frac{W}{L}\right)}}$$

Substituting in g_m

$$g_m = k_n'\left(\frac{W}{L}\right)\sqrt{\frac{2i_D}{k_n'\left(\frac{W}{L}\right)}}$$

$$= \sqrt{2k_n'\left(\frac{W}{L}\right) i_D}$$

Small signal transconductance

$$g_m = k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t) \quad \text{——(1)}$$

$$g_m = \frac{2 I_D}{V_{GS} - V_t} \quad \text{——(2)}$$

$$g_m = \sqrt{2k_n'} \cdot \sqrt{\frac{W}{L}} \sqrt{I_D}$$

The T equivalent circuit model.

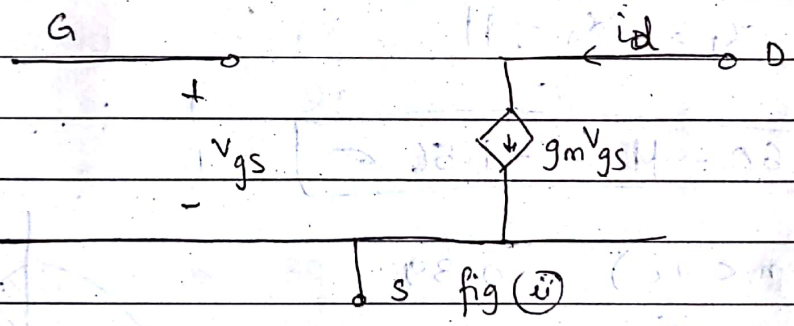
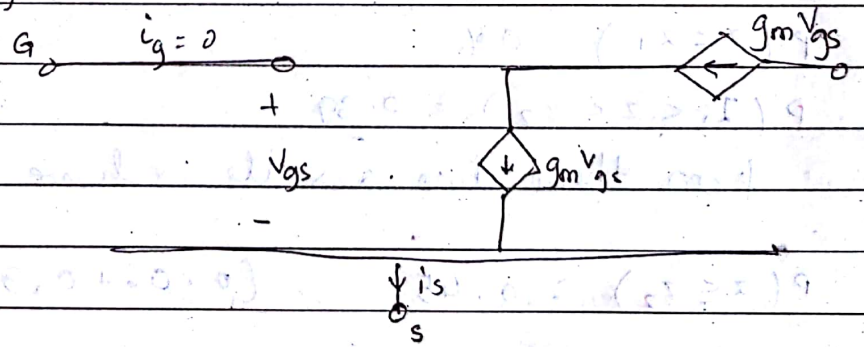


fig (ii)

Adding a 2nd current source.

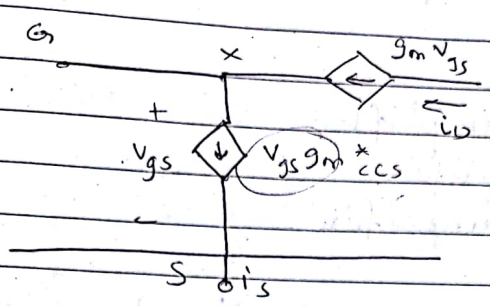


This is not affecting only D terminal characteristics

fig (b)

* Control current source

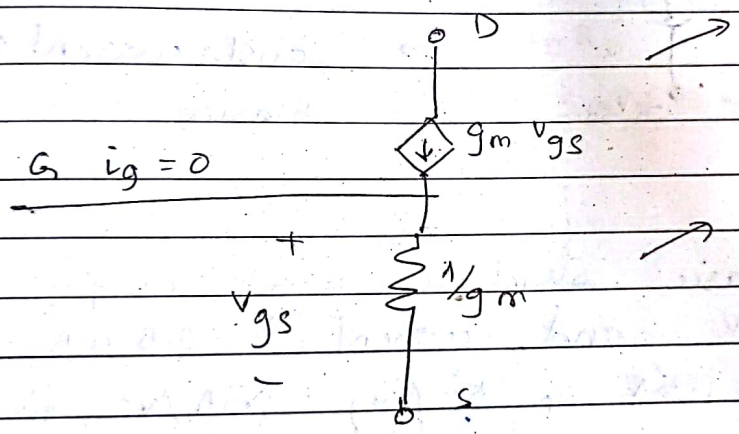
③ gate & load are current



This also won't affect anything.

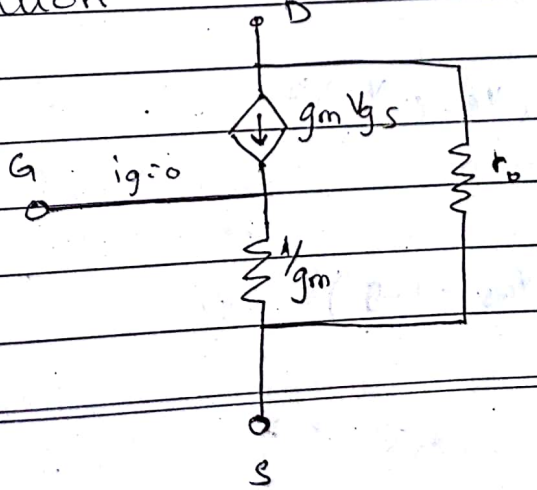
④ Turning the above model & replacing the control i source by a resistance

T-model.



$$\frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m}$$

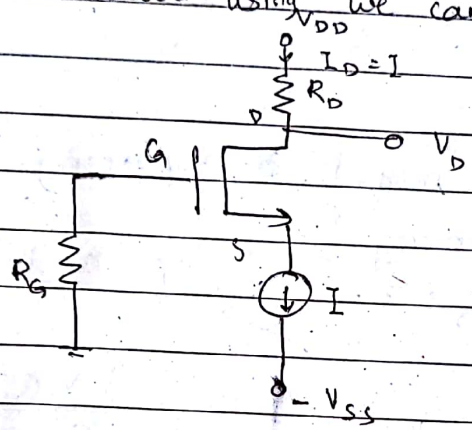
T-equivalent model considering channel length modulation



Single stage MOS amplifiers

- Common Source amplifier
- Common Gate amplifier
- Common drain amplifier

Basic structure using we can build other amplifier.



→ const current source biasing

Ex: Consider the basic structure given in fig where $V_{DD} = -V_{SS} = 10V$ and current $i = 0.5\ mA$, $R_G = 4.7M$ $R_D = 15\ K\Omega$, $V_t = 1.5\ V$ & $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$, find the values of V_{OV}, V_{GS}, V_G, V_S and V_D, also calc values of g_m and r_o assuming $V_A = 75\ V$.

→

$$i_D = \frac{1}{2} K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$0.5m = \frac{1}{2} \cdot 1m\,(V_{GS} - 1.5)^2$$

$$V_{GS} = 2.5V$$

$$V_{OV} = V_{GS} - V_t$$

$$= 2.5 - 1.5$$

$$V_{OV} = 1V$$

$$V_G = 0V$$

$$V_{GS} = V_G - V_S$$

$$-2.5V = V_S$$

$$V_D = V_{DD} - I_D R_D$$

$$= 10 - (0.5m)(15k)$$

$$= 10 - 7.5$$

$$V_D = 2.5V$$

$$V_{DS} = V_D - V_S$$

$$V_{DS} = 2.5 - (-2.5)$$

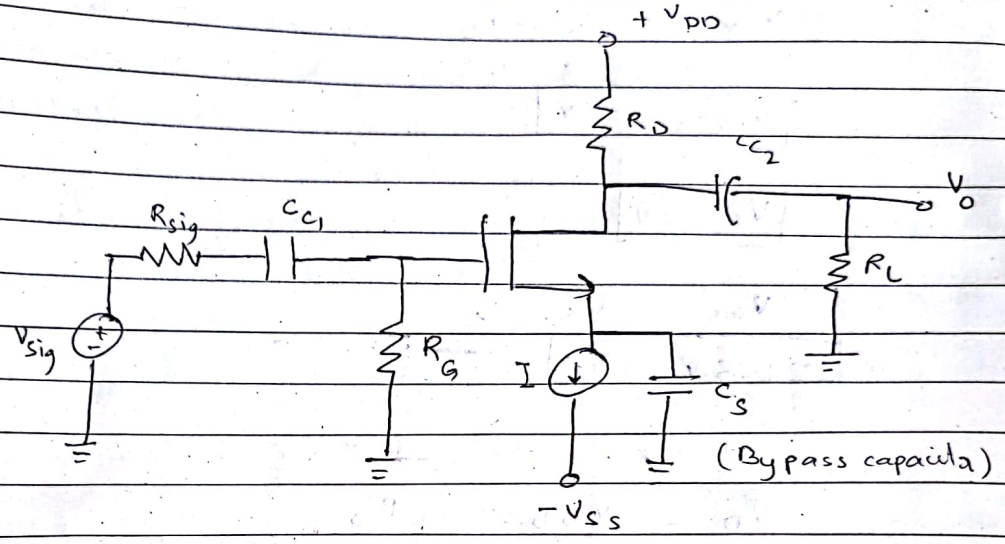
$$V_{DS} = 5V$$

(iii) $g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2(0.5)m}{2.5 - 1.5} = 1mA/V$

$r_o = \frac{V_A}{i_D}$ Early voltage

$= 150 k\Omega$ //

1) Single stage common source amplifier & derivation of the amplifier parameters.



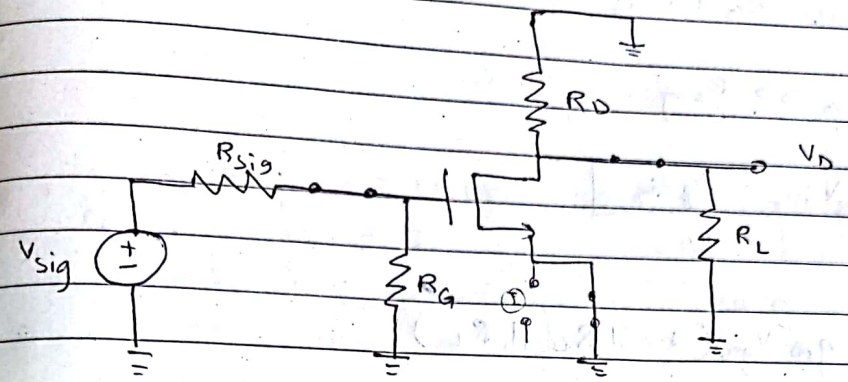
C_S impendance has to be small, so that it acts as short for ac source. So that all i flowing in source terminal will go to ground.

$$X_C = \frac{1}{2\pi f C} = \infty$$

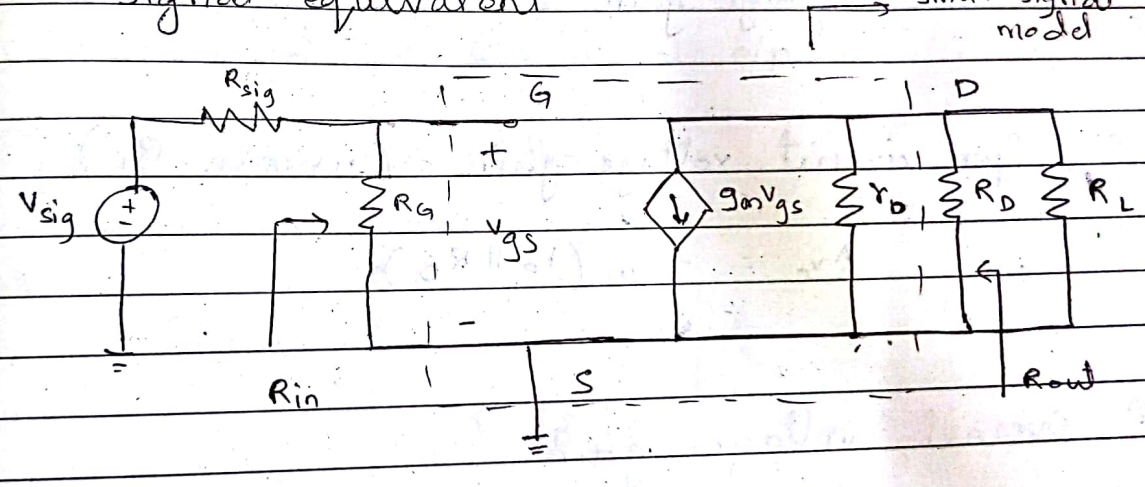
So for dc it o/c
ac it s/c

C_{C_1} & C_{C_2} are coupling capacitor.
R_{sig} is internal resistance of signal source
(A funtional equivalent will have some ~~~)
C_{C_1} & C_{C_2} allows all current to flow in ac.

AC equivalent



Small signal equivalent :-



① $R_{in} = R_G$

② $R_{out} = r_D \parallel R_D$

$r_D >> R_D$

$R_{out} = R_D$

Eg ⇒ $\frac{1M \times 1k}{1M + 1k} \simeq 1k\,\Omega$

③ $V_{in} = \frac{V_{sig} R_G}{R_G + R_{sig}}$

$R_G >> R_{sig}$

$$\boxed{V_{in} = V_{g\,sig}}$$

④ $V_o = -g_m V_{gs} (r_o \| R_D \| R_L)$

$$\boxed{A_V = \frac{V_o}{V_{gs}} = -g_m (r_o \| R_D \| R_L)}$$

voltage gain

⑤ Open circuit voltage gain (remove R_L)

$$A_{V_o} = -g_m (r_o \| R_D)$$

⑥ Overall voltage gain

$$G_V = \frac{V_o}{V_{sig}} = \frac{V_o}{V_{in}} \times \frac{V_{in}}{V_{sig}} = \frac{A_V . V_{in}}{V_{sig}}$$

From ③

$$\frac{V_{in}}{V_{sig}} = \frac{R_G}{R_G + R_{sig}}$$

$$\therefore G_V = A_V . \left(\frac{R_G}{R_G + R_{sig}} \right)$$

$$G_v = -g_m V_{gs} (r_o \| R_D \| R_L) \cdot \frac{R_G}{R_G + R_{sig}}$$

Eg: Consider common source amplifier with basic structure & with the values already solved in previous problem, find R_{in}, R_{out} & A_{vo} with & without r_o & calc. the overall voltage gain G_v with r_o taken into account when $R_{sig} = 10\,k\Omega$

$R_L = 15\,k\Omega$

$V_{sig} = 0.4\,V_{pp}$

then what is signal at o/p?

→ Consider ckt. without r_o

$R_{in} = R_G = 4.7\,M\Omega$

$R_{out} = R_D = 15\,k\Omega$

$A_{vo} = -g_m [R_D]$

$= -15$

With r_o

$R_{in} = R_G = 4.7\,M\Omega$

$R_{out} = r_o \| R_D = 13.64\,k\Omega$

$A_{vo} = -g_m [R_D \| r_o]$

$= -13.64$

Overall voltage gain

$$G_V = -g_m [R_D \parallel r_o \parallel R_L] \frac{R_G}{R_G + R_{sig}}$$

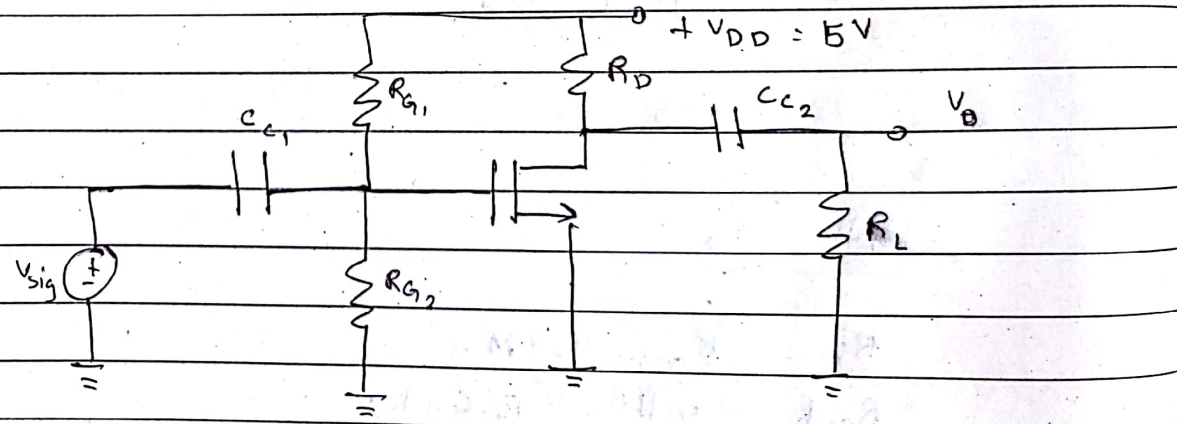
$$= -1m [+15 \parallel 150 \parallel 15k] \cdot \frac{4.7M}{4.7M + 10k}$$

$$\boxed{G_V = -7}$$

$$G_V = \frac{V_o}{V_{sig}} \qquad V_o = G_V \times V_{sig}$$

$$\boxed{V_o = -2.8V}$$

7) Determine Q-point values & voltage gain A_V for the below circuit given $R_{G_1} = 130\,M\Omega$, $R_{G_2} = 20M$, $R_D = R_L = 1M\Omega$, $V_t = 1V$, $\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right) = 10\,\mu A/V^2$



→ $V_S = 0$

$$V_G = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}}$$

$$\boxed{V_G = 2V}$$

$$\boxed{V_{GS} = 2V}$$

$$i_{DQ} = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$= 10\mu \times (2-1)^2$$

$$\boxed{i_{DQ} = 10\,\mu A \;//}$$

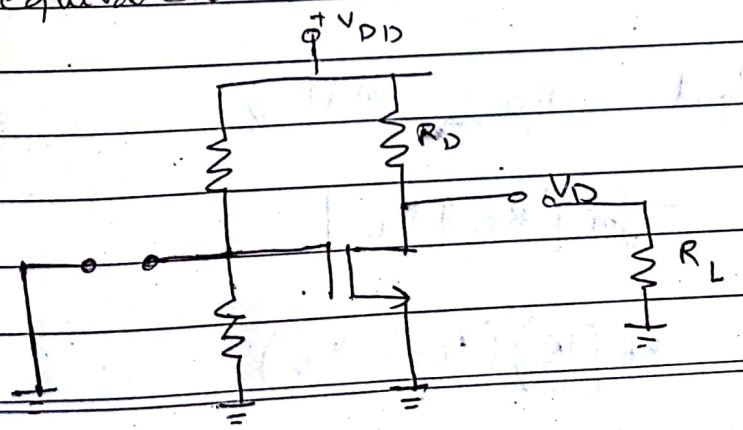
$$V_{DQ} = V_{DD} - i_D R_D$$

$$= 15 - (10\mu)\,1M$$

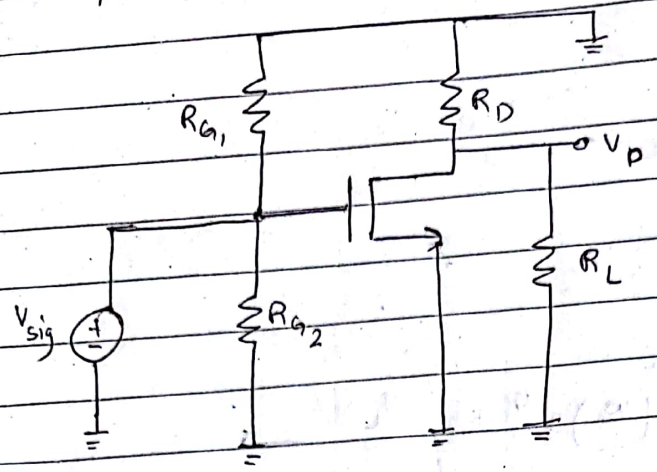
$$\boxed{V_{DQ} = 5V}$$

Draw ac eq. & small eq. to find voltage gain

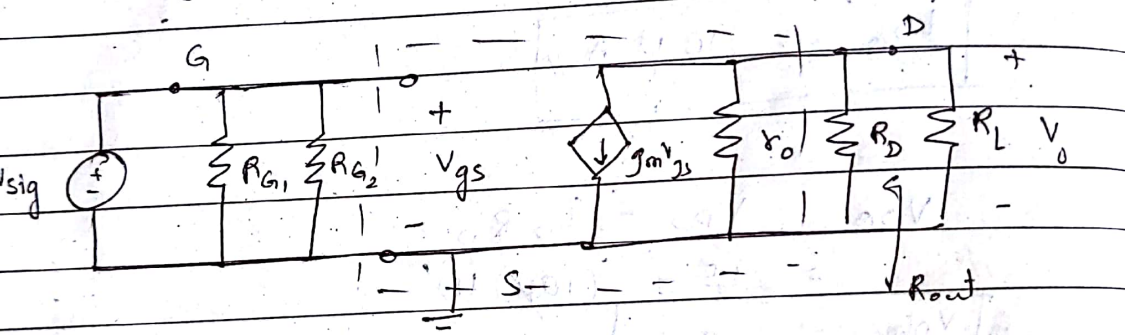
DC equivalent :



AC equivalent



Small signal model



Take r_o only if channel length modulation is considered.

→ R_{in} i/p resistance $R_{G_1} \| R_{G_2} = 130 \| 20$

$= 17.33\ M\Omega$

$R_{out} = R_D = 1M\Omega$ //

$A_v = -g_m [R_D \| R_L]$

$g_m = k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)$

$= 20\mu (2-1) = 20\mu\mho$ //

$$A_V = -20\mu \left[1 \parallel \frac{1}{\sim} \right]$$

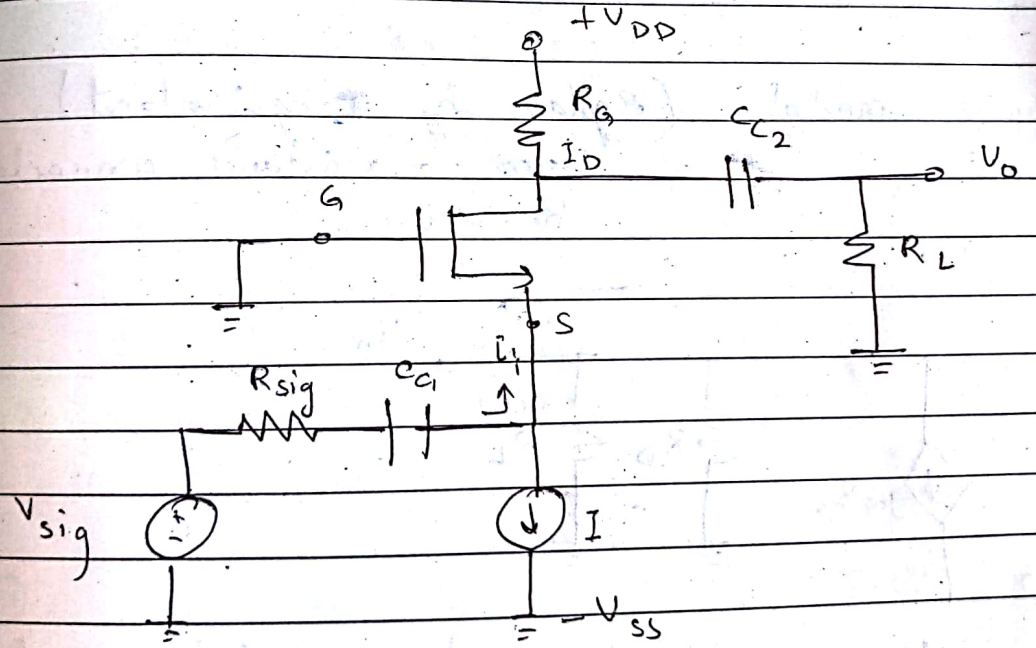
$$\approx -20\mu \left(\frac{1}{2}\right) m$$

$$\boxed{A_V \approx -10}$$

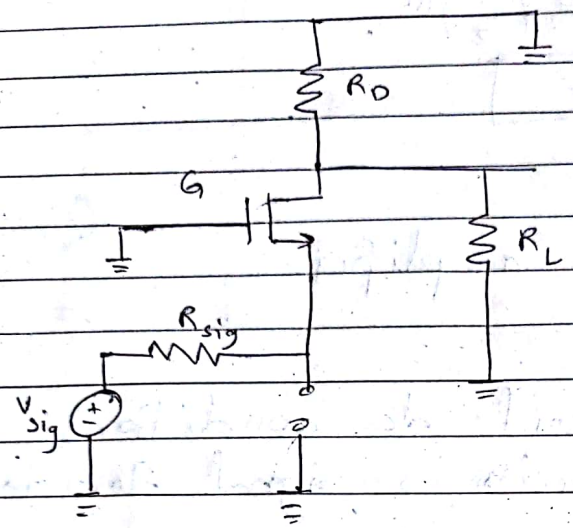
The common gate amplifier

C_{C_1} & C_{C_2} to avoid dc conditions

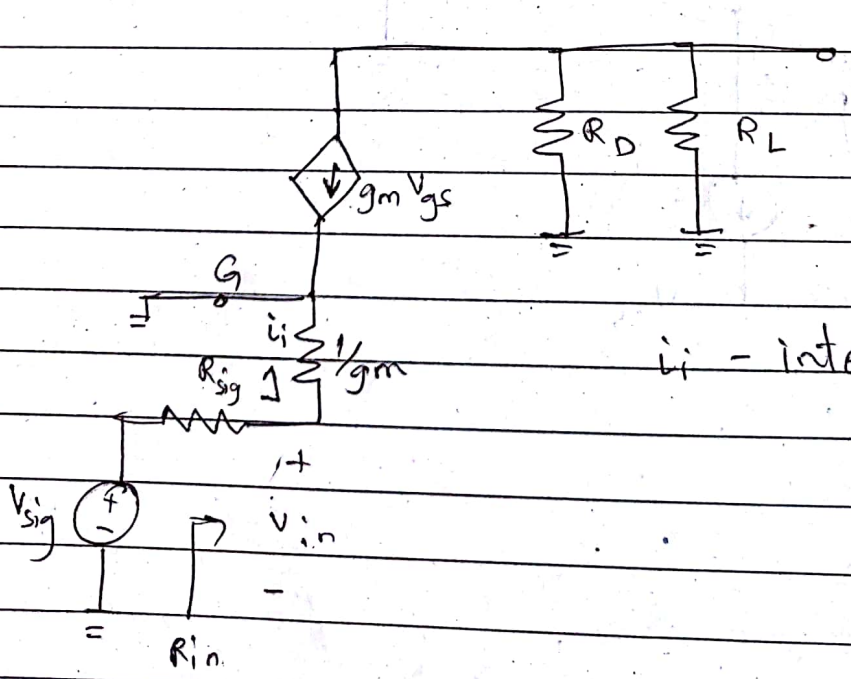
No bypass capacitor as signal flow to ground



AC equivalent



Small signal model (Replace by π-equivalent)
since a resistance connected to source.



i_i - intermediate current

Derivation of amplifier parameters

① $R_{in} = \frac{1}{g_m}$

② $R_{out} = R_D$

$$v_{in} = \frac{V_{sig} \times R_{in}}{R_{in} + R_{sig}}$$

$$R_{in} = \frac{1}{g_m}$$

③ $$v_{in} = \frac{V_{sig} \times 1/g_m}{1/g_m + R_{sig}}$$

$R_{sig} << 1/g_m$ for $\boxed{v_{in} = V_{sig}}$

$$\therefore \quad v_{in} = \frac{V_{sig}}{1 + g_m R_{sig}}$$

④ $i_o = i_D = i_i$ —— (A)

$$+i_1 = \frac{+v_{in}}{1/g_m} = g_m v_{gs}$$ —— (A)(A)

$$\boxed{i_d = -i_1 = -g_m v_{gs}}$$

$$v_o = -i_d (R_D \parallel R_L)$$

$$= g_m v_{gs} (R_D \parallel R_L)$$

$$A_V = \frac{v_o}{v_{gs}} = g_m (R_D \parallel R_L)$$

$$A_{v_0} = g_m R_D$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_o}{v_{in}} \times \frac{v_{in}}{v_{sig}}$$

$$= A_v \times \frac{v_{in}}{v_{sig}}$$

$$G_v = g_m [R_D \| R_L] \frac{1}{1 + g_m R_{sig}}$$

Ex: In a CG amplifier with same basic struct & g_m = ~~1mA/V²~~ , $R_D = 15\,k\Omega$, determine R_{in}, R_{out}, A_v, A_{v_0} & G_v for $R_L = 15\,k\Omega$ & $R_{sig} = 50\,\Omega$.
What will be the overall voltage gain for $R_{sig} = 1k\Omega$, $10\,k\Omega$ & $100\,k\Omega$

→ Ans: $R_{in} = 1k\Omega$
$R_{out} = 15\,k\Omega$
$A_v = 7.5$
& $G_v = 7.14$
$A_{v_0} = 15$
$R_{sig} = 1k\Omega$
$G_v = 3.75$
$R_{sig} = 10\,k\Omega$
$G_v = 0.682$
$R_{sig} = 100\,k\Omega$
$G_v = 0.07493$