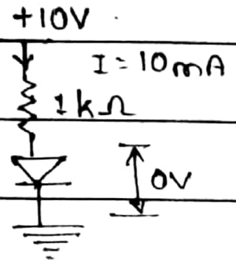
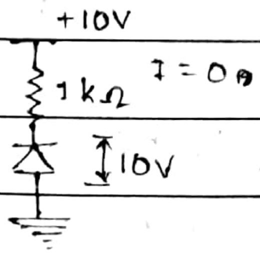
unit-01

chap 01 : Diode modeling and applications.





$V = IR$

Ideal diode : Forward bias - short circuit

Reverse bias - open circuit

$$\boxed{I_D = I_S\, e^{(v_D / nV_T)}} \quad \text{--- (A)}$$

I_D = diode current

v_D = diode voltage

$n = 1$ or 2

V_T = Thermal voltage = 25mV at room temp.

$$\boxed{V_T = \frac{kT}{q}}$$

I_S: Saturation or Scaling current (order of 10^{-15}A)

Let us assume that a diode ~~carrys~~ carries current I_{D1} when it's voltage is V_{D1} under forward bias conditions. Let us say changed current of I_{D2}. Thro. that diode when it's volt is V_{D2}. Let us use eqn 'A' for this connection.

Date : / /
Page No.:

$$I_{D1} = I_s \cdot e^{v_{D1}/n \cdot V_T} \quad \text{——} \ (1)$$

lly.

$$I_{D2} = I_s \cdot e^{v_{D2}/n \cdot V_T} \quad \text{——} \ (2)$$

(2) ÷ (1)

$$\frac{I_{D2}}{I_{D1}} = \frac{\cancel{I_s} \cdot e^{V_{D2}/nV_T}}{\cancel{I_s} \cdot e^{V_{D1}/nV_T}} \quad \text{——} \ (3)$$

$$\ln \frac{I_{D2}}{I_{D1}} = \frac{v_{D2} - v_{D1}}{nV_T} \quad \text{——} \ (4)$$

$$v_{D2} - v_{D1} = nV_T \ln \frac{I_{D2}}{I_{D1}} \quad \text{——} \ (5)$$

$$\boxed{v_{D2} - v_{D1} = 2.3 n V_T \log_{10} \frac{I_{D2}}{I_{D1}}} \text{ volts} \quad \text{——} \ (6)$$

when there is decade change in the current for ex. when $I_{D1} = 1mA$ then $I_{D2} = 10mA$. substituting this in above eqn. we have change in diode voltage.

$$\boxed{v_{D2} - v_{D1} = 2.3 n V_T \cdot 1}$$

$$\boxed{\Delta V_D = V_{D2} - V_{D1} = 2.3 n V_T} \quad \text{——} \ (7)$$

eqn (7) shows change in diode voltage when there is decade change in the current.

While designing diode ~~suffer~~ sobber this term will be given as one of it's specification of the diode.

10/08/2017

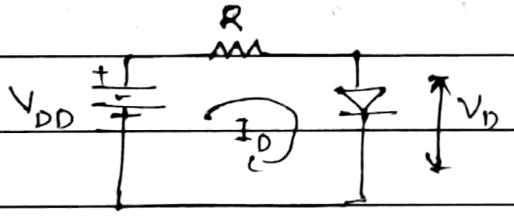
Date : / /
Page No.:

Diode Models:

1. An exponential model → Graphical method
   → Iterative method.
2. Piece-wise linear model
3. constant voltage drop or 0.7V drop model.
4. An ideal diode model.
5. Small-signal model.

1. Exponential model. (Accurate model).

$$I_D = I_S e^{v_D/nV_T} \quad \text{—— (1)}$$



(1)(a)

$$v_{DD} = I_D R + v_D \quad \text{—— (2)}$$

$$\boxed{I_D = \frac{v_{DD} - v_D}{R}} \quad \text{—— (3)}$$

a) Graphical methode

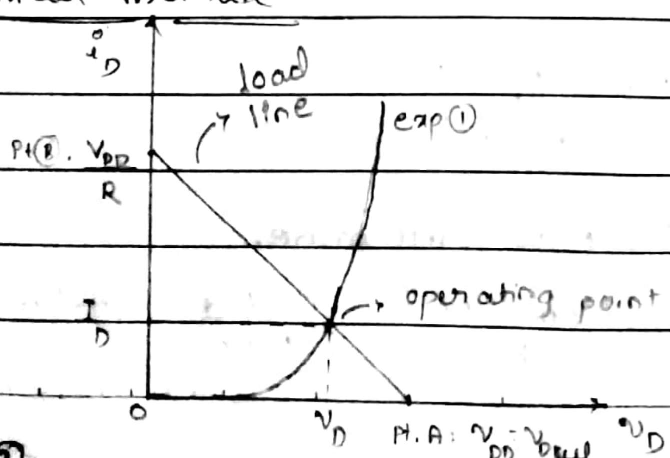


Fig 1(B).

Date : / /
Page No.:

consider eqn 3

Let, $I_D = 0$.

$v_{D_{cut}} = v_{DD} \longrightarrow$ pt (A)

let $v_D = 0$.

$I_{D_{sat}} = \dfrac{V_{DD}}{R} \longrightarrow$ pt (B)

} DC load line.

b) ~~Iterative method~~:

for complex circuit graphical method of determining V_D & I_D will be tidious & hence this graphical methode is used only for simple circuit.

b) Iterative method:

Ex : 1) Determine the current I_D & the diode volt. V_D for the circuit shown in fig 1A. when $V_{DD} = 5V$ & $R = 1k\Omega$, assume that diode has the current of 1mA. At a voltage of 0.7V. and it's volt. drop changes by 0.1V. for every decade change in current

Sol^n:

$v_{DD} = 5V$, $R = 1k\Omega$, $v_{D_1} = 0.7V$, $I_{D_1} = 1mA$.

$v_D = ?$, $I_D = ?$

using eqn 3. let us determine.

$$I_{D_2} = \frac{v_{DD} - v_{D1}}{R} = \frac{5 - 0.7}{1000} = 4.3mA.$$

Date : / /
Page No.:

wkt. ($2.3nV_T = 0.1V/decade$)

$$V_{D2} - V_{D1} = 2.3\, nV_T \log \frac{I_{D2}}{I_{D1}}$$

$$V_{D2} = \cancel{0.}\, V_{D1} + 0.1 \times \log \frac{4.3mA}{1mA}$$

$$= 0.7 + 0.063$$

$$\therefore \boxed{V_{D2} = 0.763\,V}$$

Note: (*) comparing I_{D1} & I_{D2} values. as a diff. is more one ~~of~~ more iteration is req.

2nd iteration: $I_{D2}' = \frac{V_{DD} - V_{D2}}{R}$

$$= \frac{5 - 0.763}{1000} = \boxed{4.237\, mA}$$

$$V_{D2}' - V_{D2} = \cancel{0.1 \times \log}\ 2.3nV_T \log \frac{I_{D2}'}{I_{D2}}$$

$$\therefore V_{D2}' = V_{D2} + 2.3nV_T \log \frac{I_{D2}'}{I_{D2}}$$

$$V_{D2}' = 0.763 + 0.1 \times \log\left(\frac{4.237}{4.3}\right)$$

$$\boxed{V_{D2}' = 0.762\,V.}$$

(*) comparing the values of I_D & V_D. of 1st & 2nd iteratio-n. we can say that. diff. is less hence. we can

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Date : / /
Page No.:

consider the results of 2^{nd} iteration as final values of I_D & V_D for the circuit shown

$$\therefore \boxed{\begin{aligned} V_D &= 0.762V \; \& \\ I_D &= 4.237mA. \end{aligned}}$$

*. This iterative method of determining ideal V_D will be tidious one when no. of iterations are more naturally for complex circuit no. of iteration will increase & hence this method is useful. only for simple circuits where no. of iterations are less and we can get accurate values of V_D & I_D.

2. Piece-wise linear model:

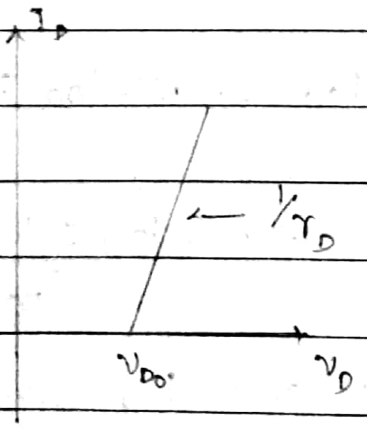


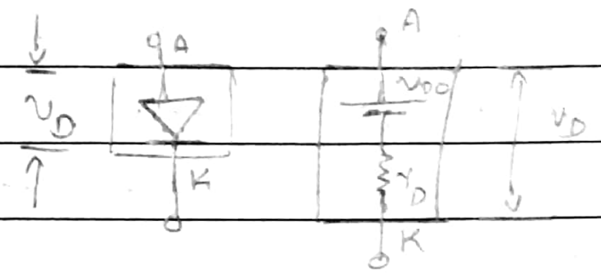
fig ② ⓐ V-I characteristics

*. where $V_{Do} = V_\gamma$ = cut-in voltage of the diode.

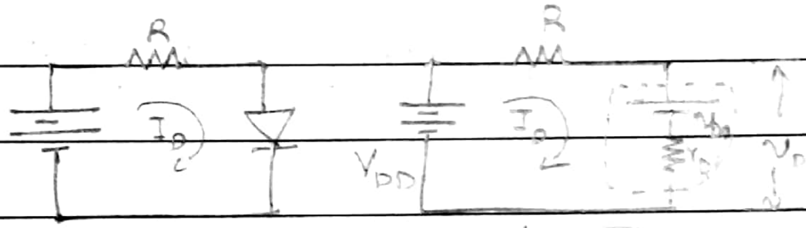
r_D = forward resistance.

Date : / /
Page No.:

fig 2 (b) piece-wise linear model.



considering the circuit of fig 1 (a)



$$\boxed{v_D = v_{D0} + I_D r_D} \quad \text{— (1)}$$

fig 2c

Applying KVL to fig 2c

$$v_{DD} = I_D R + v_{D0} + I_D r_D \quad \text{— (a)}$$

$$v_{DD} = I_D (R + r_D) + v_{D0} \quad \text{— (b)}$$

$$\boxed{I_D = \frac{V_{DD} - v_{D0}}{(R + r_D)}} \quad \text{— (c)}$$

Ex. considering the ex. taken in the previous model let us determine ideal v_D values when piece-wise linear model parameters are given as. $v_{D0} = 0.65\,V$, $r_D = 20\,\Omega$.

Solⁿ:

$$I_D = \frac{5 - 0.65}{1000 + 20}$$

$$\boxed{I_D = 4.26\,mA.}$$

$$v_D = v_{D0} + I_D r_D$$

$$= 0.65 + (4.26 \times 10^{-3})(20) = 0.735\,V$$

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11/08/2017

Date : / /

Page No.:

*. comparing I_D & V_D values of piece-wise linear model with iterative analysis. we can say that diff. is less and result of the approx. analysis which is piece wise linear model analysis is better comparing with the iterative analysis.

③. Constant voltage drop volt. model or. 0.7V model.

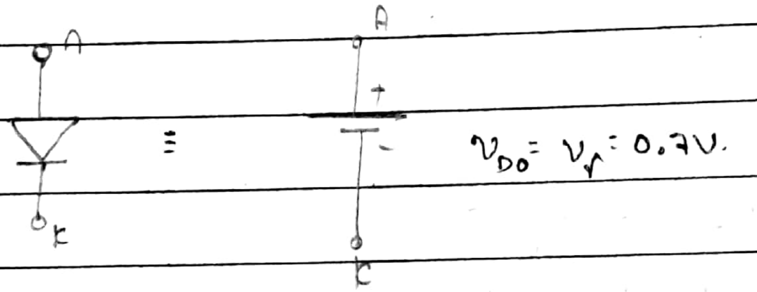
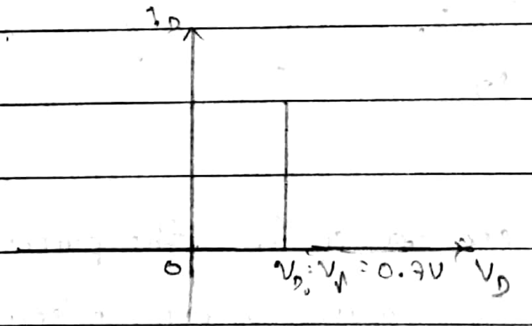
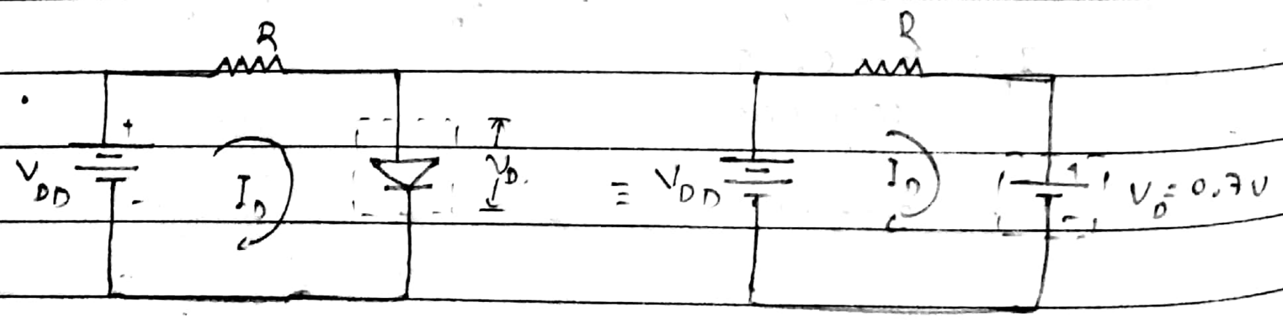


Fig ③ ⓐ.



③ ⓑ vi. char.



Date : / /
Page No.:

$$\boxed{* \; I_D = \frac{V_{DD} - V_D}{R}}$$

consider, same ex. which has taken from the 1st model but it should be noted that under specif-ication of const. volt of 0.7V has to be given then it self will be diode volt. V_D' and corresponding current can be determined using eqn.

$$I_D = \frac{V_{DD} - V_D}{R}$$

Hence, diode volt. and diode currents are.

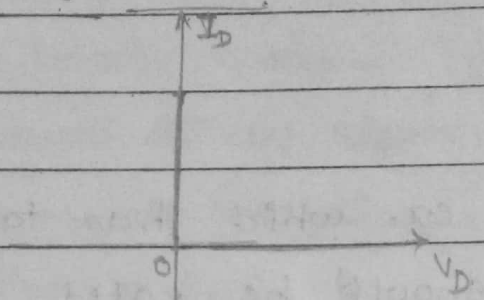
$V_D = 0.7V$ (const).

$I_D = 4.3mA$.

$$\boxed{\begin{aligned} V_{D0} &= 0.7V = V_D. \\ I_D &= \frac{V_{DD} - V_{D0}}{R} = \frac{5-0.7}{1000} = 4.3mA. \end{aligned}}$$

* comparing these results in the previous models we can say that these are not too diff. from the values obtained from previous models.

4. Ideal diode model.



VI char.

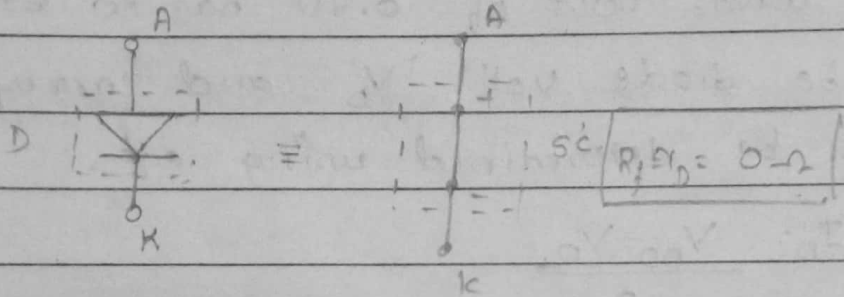
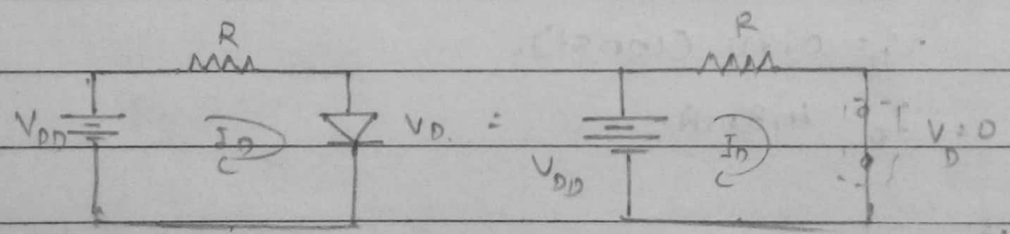


Fig 4 (a)



*. $I_D = \dfrac{V_{DD} - V_D}{R} = \dfrac{5}{1k} = 5\,mA.$

here $\boxed{V_D = 0\,V}$

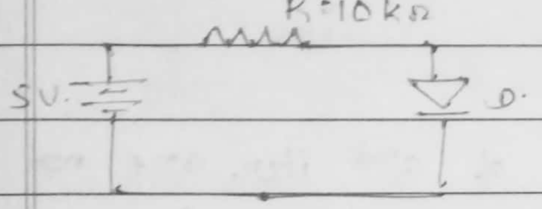
Problems.

1. For from the follo. circuit determine the values of I_D & V_D when $V_{DD} = 5V$, and $R = 10k\Omega$ assume that diode has the voltage of $0.7V$ at $1mA$ current. and the voltage changes by $0.1V$/decade current change

use (a) Integration methode.

(b) Piece wise linea model with $V_{D0} = 0.65V$
& $r_D = 20\Omega$.

(c) const. volt. drop model with $V_D = 0.7V$.



Sol^n. (a) Iterative method.:

$V_{D1} = 0.7V$, $I_{D1} = 1mA$.

1st iteration

$$I_{D2} = \frac{V_D - V_{D1}}{R} = \frac{5-0.7}{10k\Omega} = 0.43mA.$$

$$V_{D2} - V_{D1} = 2.3nV_T \log \frac{I_{D2}}{I_{D1}} =$$

$$V_{D2} - 0.7 = (0.1)\log\left(\frac{0.43\times10^{-3}}{1\times10^{-3}}\right)$$

$$\boxed{V_{D2} = 0.6633V.}$$

~~2nd~~ as ~~current~~ values of I_{D2} & V_{D2} are much diff. from the values of I_{D1} & V_{D1}. Hence 2nd iteration is required.

2nd iteration:

$$I'_{D2} = \frac{V_{DD} - V_{D2}}{R} = \frac{5-0.6633}{10000} = 0.4337mA.$$

Date : / /
Page No.:

$$V_{D2}' = V_{D2}^{0} + 2.3 n V_T \log\left(\frac{I_{D2}'}{I_{D2}}\right)$$

$$= 0.6633 + (0.1) \log$$

$$\boxed{V_{D2}' = 0.6636\ V}$$

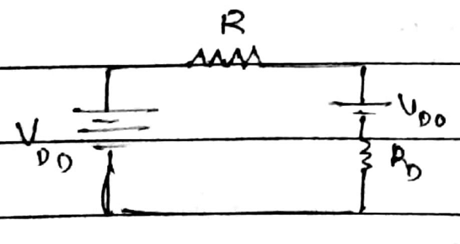
as values of I_{D2} & V_{D2} of 2nd iter. are not much diff from the values obtained from 1st iteration we can consider V_{D2}' & I_{D_2}' as the final values of diode volt. & current.

ie $\boxed{V_D = 0.6636\ V}$

$\boxed{I_D = 0.4337\ mA}$

(b) piece-wise.

$V_{D0} = 0.65\ V$, $R_D = 20\ \Omega$.



$$I_D = \frac{V_{DD} - V_{D0}}{(R + R_D)}$$

$$= \frac{5 - 0.65}{10\,k\Omega + 20}$$

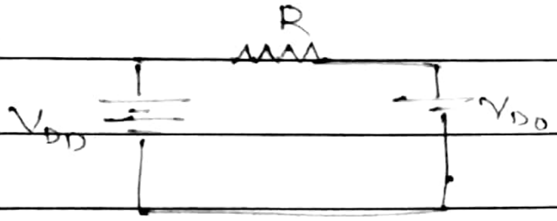
$$= 0.434\ mA$$

$V_D = V_{D0} + I_D R_D$

$= 0.65 + (0.434 \times 10^{-3})(20)$

$\boxed{V_D = 0.6587\,\Omega}$

(c)



$V_{D0} = 0.7V.$

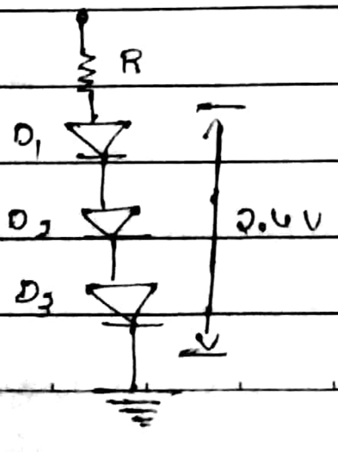
$\cancel{V_D}.\quad I_D = \frac{V_{DD} - V_{D0}}{R} = \frac{5 - 0.7}{10K\Omega}$

$\boxed{= 0.43mA.}$

$\cancel{V_D = 0.7 + (0.43 \times 10^{-3})}$

$\boxed{V_D = 0.7V}$

(2) Design the follo. circuit to provide an o/p volt. of 2.4 V. assume that the diodes available have 0.7 V drop at 1mA current and $\Delta V = 0.1$ V/decade current change.



Date : / /
Page No.:

Sol^n. $V_{D1} = 0.7V$, $I_{D1} = 1mA$. $\Delta V = 2.3nV_T = 0.1$

$V_{D2} = \frac{V_o}{3} = \frac{2.4}{3} = 0.8V.$

$V_{D2} - V_{D1} = 2.3nV_T \log \frac{I_{D2}}{I_{D1}}$

$(0.8 - 0.7) = 0.1 \log \frac{I_{D2}}{I_{D1}}$

$0.1 = 0.1 \log \frac{I_{D2}}{I_{D1}}$

$10 = \frac{I_{D2}}{1 \times mA}$

$\boxed{I_{D2} = 10mA}$

Let V_R be the volt. accross the resistor.

$V_R = 10 - V_o = 10 - 2.4$

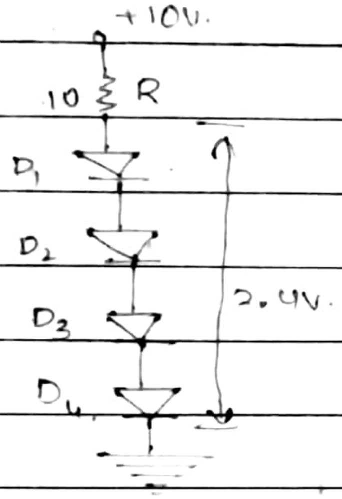
$= 7.6. V$ //

$R = \frac{V_R}{I_{D2}} = \frac{7.6}{10mA} = 760\Omega$ // or : $0.76 k\Omega$

Date : / /
Page No.:

4.4ω

3) +10V.



Sol^n. $V_{D1} = 0.7V$, $I_{D1} = 1mA$. $\Delta V_D = 2.3nV_T = 0.1$

$V_{D2} = \frac{V_0}{4} = \frac{2.4}{3} = 0.6V$.

$V_{D2} - V_{D1} = 2.3nV_T \log \frac{I_{D2}}{I_{D1}}$

$0.6 - 0.7 = 0.1 \log \frac{I_{D2}}{I_{D1}}$

$-1 = \log \frac{I_{D2}}{I_{D1}}$

$\boxed{I_{D2} = \cancel{0.01}\, 0.1mA}$

$V_R = 10 - V_D = 10 - 2.4$

$= 7.6V$.

$R = \frac{V_R}{I_{D2}} = \frac{7.6}{0.1mA} = 76k\Omega$

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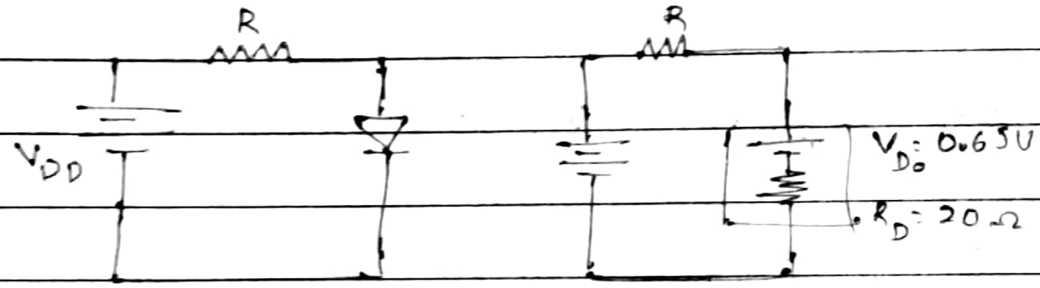
Date : / /
Page No.:

14/08/17

1) conside the diode shown in follo fig. as junction area 100x larger than diode which are being used in the previous case where $V_{D0} = 0.65V$ & $R_D = 20\Omega$. If we approx. characteristic such a way that current is increasing 100x then how are the model parameters V_{D0} & R_D will change.



Sol^n : $V_{D0} = 0.65V$, $R_D = 20\Omega$.

$V = IR$

$V_{D0} = 0.65$

$r_D' = \frac{r_D}{100} = \frac{20}{100}$

$= 0.2\Omega$

As per the data given increased jn. area of 2nd area will decrease it's resistance let us denote this resis. by r_D' and he said that VI chara. is in such a way that it's current carrying capacity is also increased by 100x hence as per this diagram using ohm's law $V = RI$. cut-in volt. V_{D0}' will remain same as V_{D0} but

$r_D' = \frac{R_D}{100} = \frac{20}{100} = 0.2\Omega$

5) Small signal model of the diode:

when a diode is used in a circuit with the dc bias. along with an AC signal which has been super imposed on this DC then for this AC signal the equ. model of the diode. when signal variation is small is called as small signal model of diode.

Before determining this small signal model the dc model. i.e 0.7V model is used here for simplicity. The circuit dia. is shown in below fig & corresponding vs charac. is also shown in follo. fig. along with small signal.

For simplicity the series resistance 'R' is not considered in the follo. circuit.

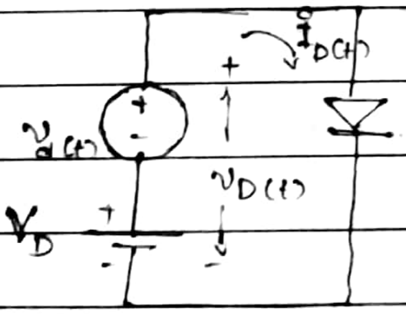


fig (1a)

V_D - dc diode voltage

$v_{d(t)}$ - AC (inst) signal

$v_{D(t)}$ = total instantaneous

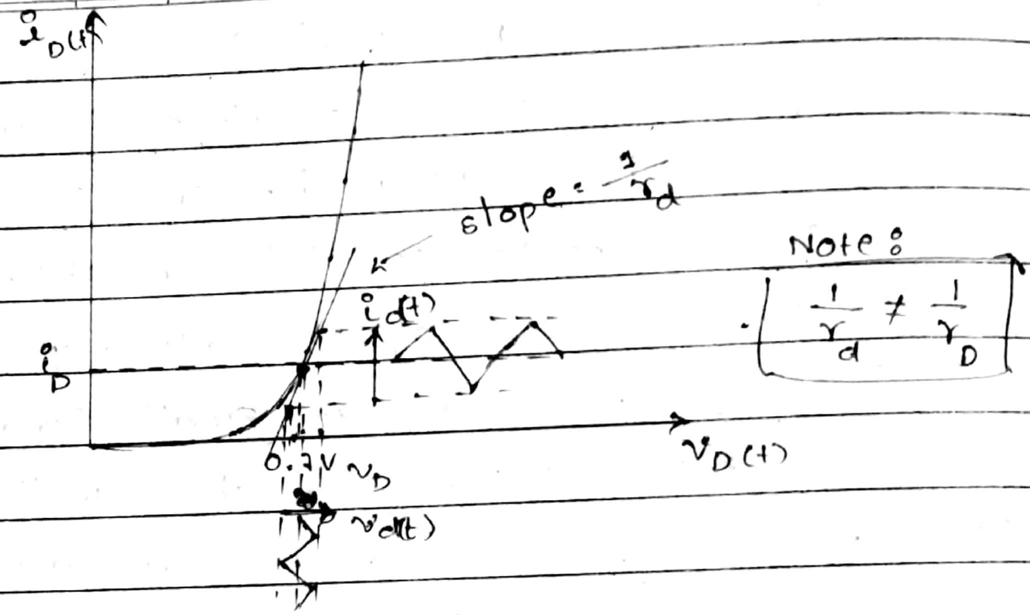
i.e $v_{D(t)} = V_D + v_{d(t)}$ —— (1)

in the absence of instantaneous small signal $v_{d(t)}$ i.e $v_{d(t)} = 0$.

then volt. V_D appears across the diode and this will be the dc volt. of the diode.

r_d: ac resis.
r_D: DC resis.

Date: / /
Page No.:



Small signal analysis:

w.k.t

$$I_D = I_S e^{V_D/nV_T} \longrightarrow ①$$

v_D total inst. diode volt.

$$v_{D(t)} = V_D + v_{d(t)} \longrightarrow ②$$

then.

total instantaneous diode current.

$$i_{D(t)} = I_S e^{v_{D(t)}/nV_T} \longrightarrow ③$$

Substituting ② to ③

$$i_{D(t)} = I_S e^{\{V_D + v_{d(t)}\}/nV_T}.$$

$$= I_S e^{V_D/nV_T} \times e^{v_{d(t)}/nV_T}.$$

$$i_{D(t)} = I_D e^{v_{d(t)}/nV_T} \longrightarrow ④$$

let us consider the term $e^{v_{d(t)}/nV_T}$, expand it using Taylor's series.

Taylors series: $e^x = 1 + \frac{x}{1!} + \frac{x^2}{2!} \ldots$

Date: / /
Page No.:

$$e^{v_{d(t)}/nV_T} = 1 + \frac{v_{d(t)}/nV_T}{1!} + \frac{\{v_{d(t)}/nV_T\}^2}{2!} + \ldots$$

in this case instantaneous signal $v_{d(t)}$ is a small signal for ex. say $v_{d(t)} = 0.01$ V. then in the taylor's expansion when square of this term is taken it's value will be neglegeble hence we neglect square term in this series so that.

$$\boxed{e^{v_{d(t)}/nV_T} = 1 + \frac{v_{d(t)}}{nV_T}} \quad \text{— (6)}$$

substituting (6) & (5) we get.

$$i_{d(t)} : \boxed{i_{D(t)} = I_D \left\{ 1 + \frac{v_{d(t)}}{nV_T} \right\}} \quad \text{— (7)}$$

$$i_{D(t)} = I_D + i_{d(t)} \quad \text{— (8)}$$

considering 2^{nd} term of eqn (7) & (8)

$$\text{i.e. } i_{d(t)} = \frac{I_D \cdot v_{d(t)}}{nV_T} \quad \text{— (9)}$$

$$\therefore \boxed{\frac{i_{d(t)}}{v_{d(t)}} = g_m : \text{small signal conductance of the diode} = \frac{I_D}{nV_T}} \quad \text{— (A)}$$

lly.

$$\boxed{\frac{v_{d(t)}}{i_{d(t)}} = \frac{1}{g_m} : r_d : \text{Small signal resistance of the diode} = \frac{nV_T}{I_D}} \quad \text{— (B)}$$

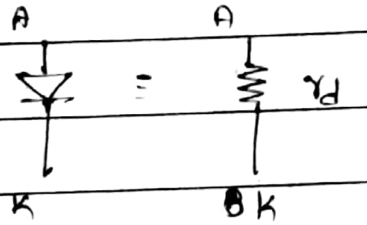
Date : / /
Page No.:

Note: ①

As seen from eqn (B) from incrementing resistance of diode →

→ depends upon dc biase current of diode I_D along with values of n & V_T.

1) The following fig give small signal model of diode



Limitting circuits and clipping circuit.

Limitting circuits.

1. Unbiased
2. biased.

1) Unbiased clipping circuits:

In these clipping circuits reference volt. which is denoted as V_R which is external dc source connected with the diode will be zero. and it is assumed that diode has 0.7 V cut-in volt. with a forw. resistance $R_f = r_D = 0$, & $R_r = \infty$ The following are

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for these unbiased clipping ckts.

(i) Positive clipping circuit.

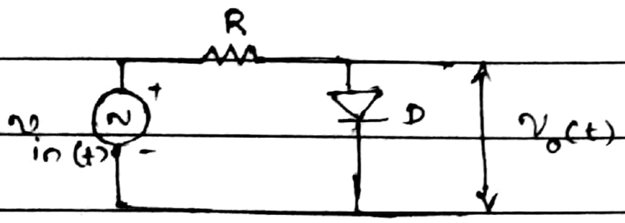
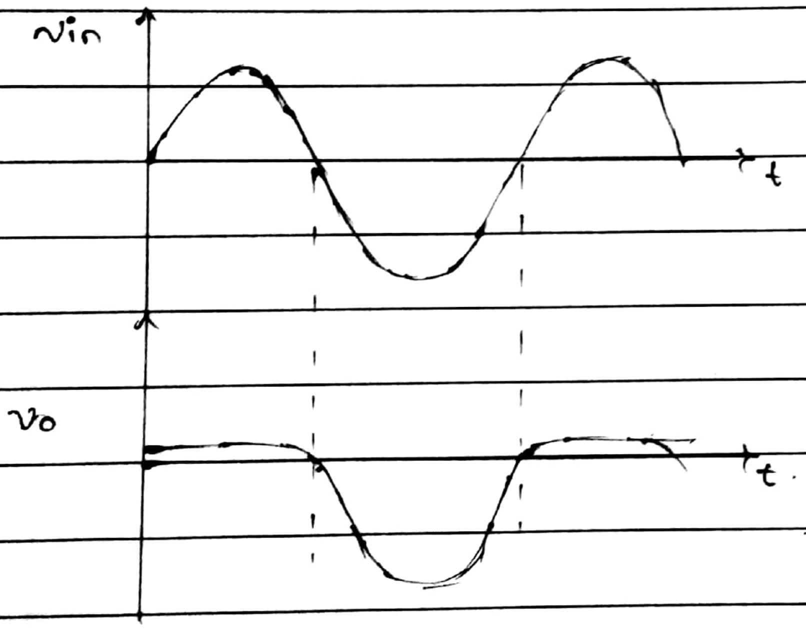
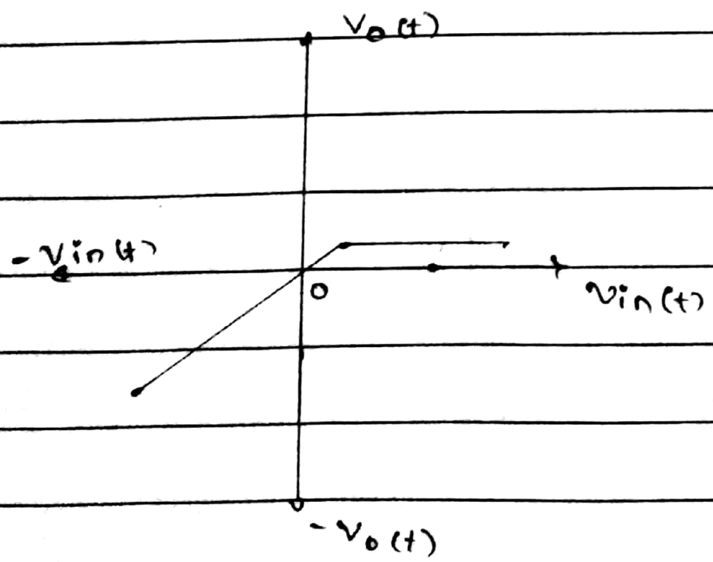


fig 1 ⓐ



i/p & o/p waveforms.



Transfer char. curve.

17/08/17

Date : / /
Page No.:

2) <u>Negative clipping circuit :</u>

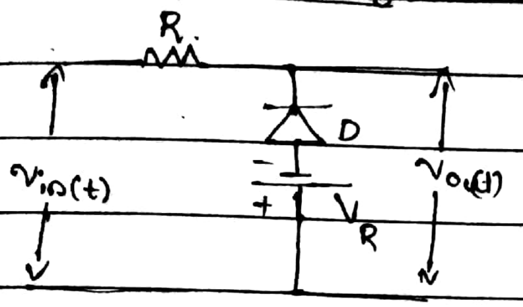


Fig 2(a)

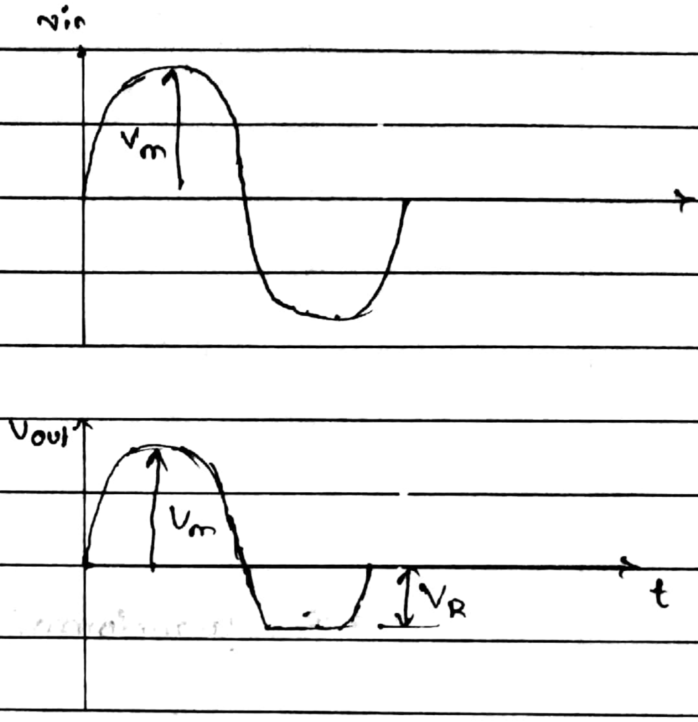
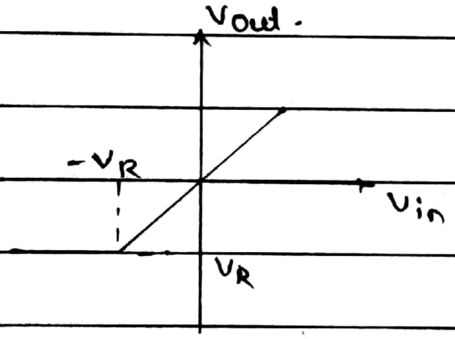
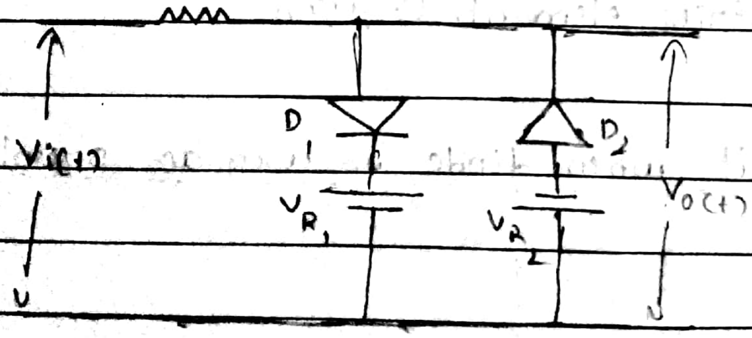


fig 2(b)

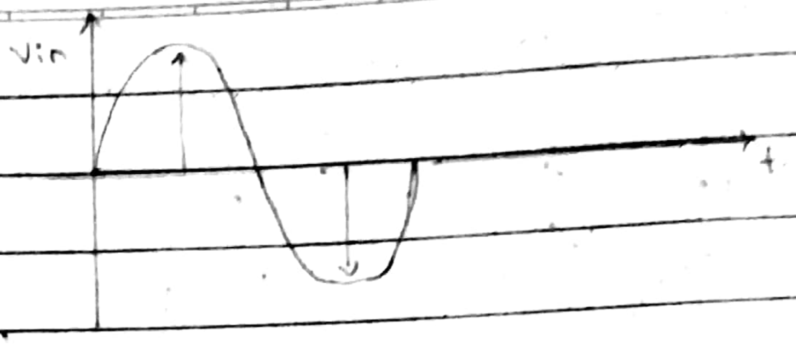


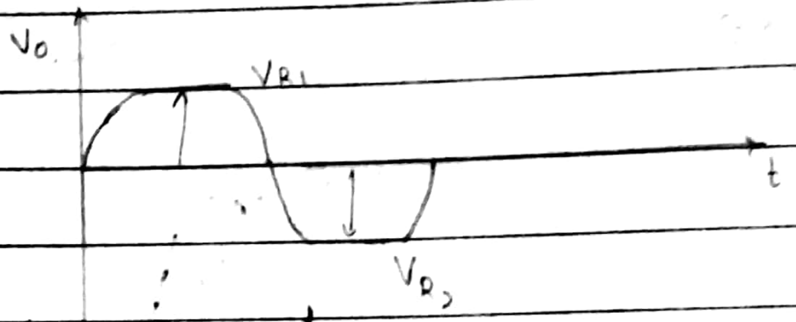
transfer characteristics.

3) <u>Combination clipping.</u>

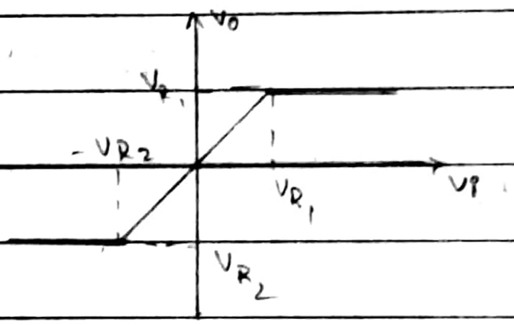


3 a





3 (b) waveforms.

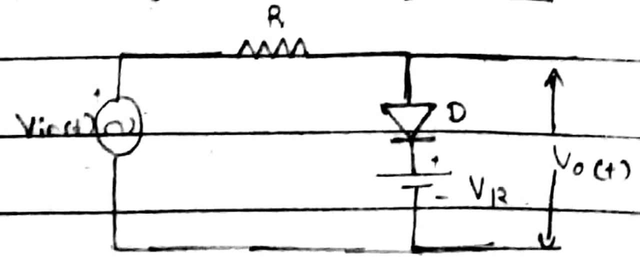


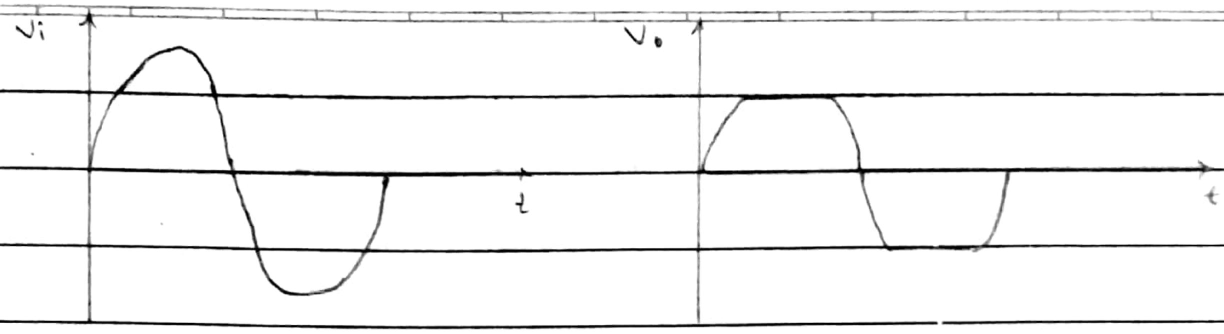
3c. transfer characteristics.

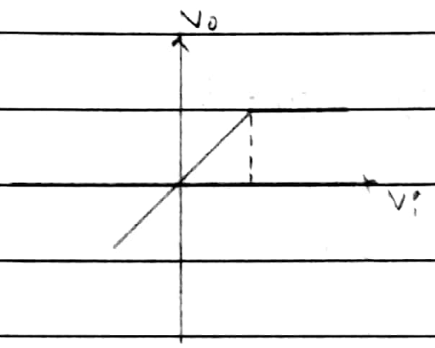
(2 circ)

Clipping circuits when diode is used as (a) shunt element and (b) ~~a~~ series element. (2 cir).

(a) Clipping circuit when diode is used as shunt element

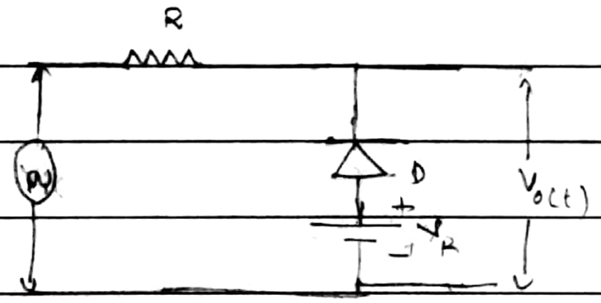
1). 

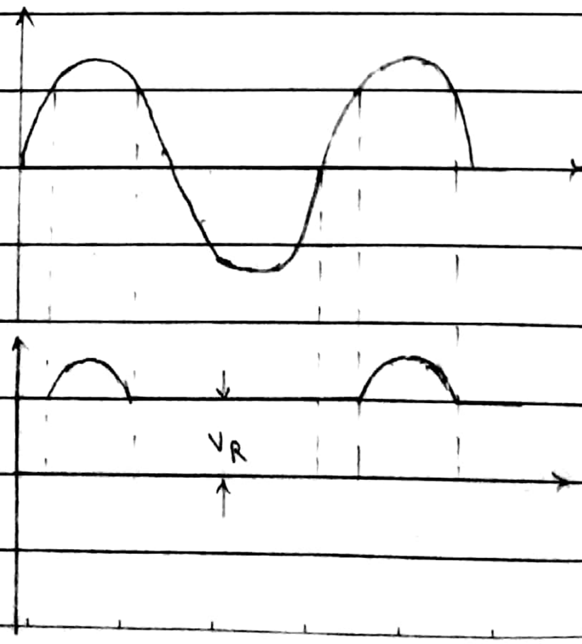




(c) transfer

2)





21/08/17

2).

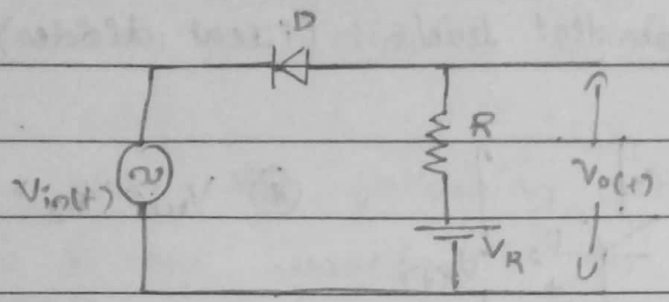
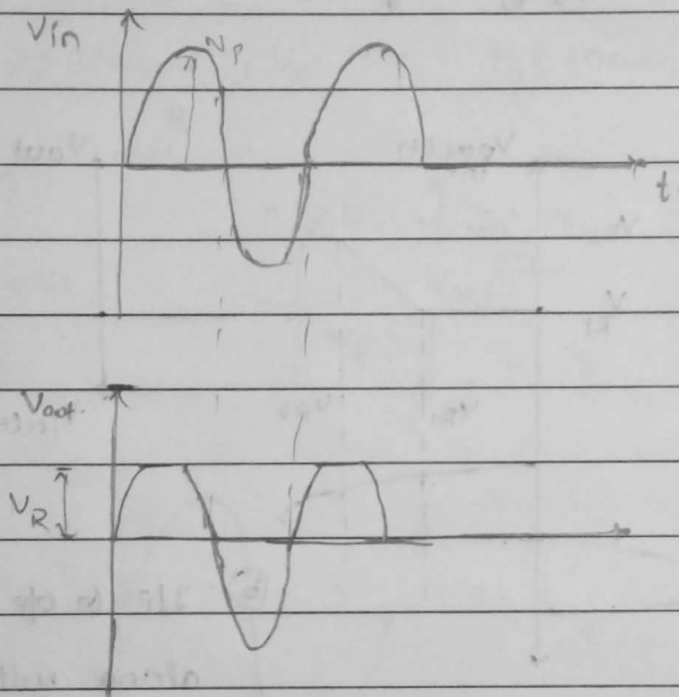
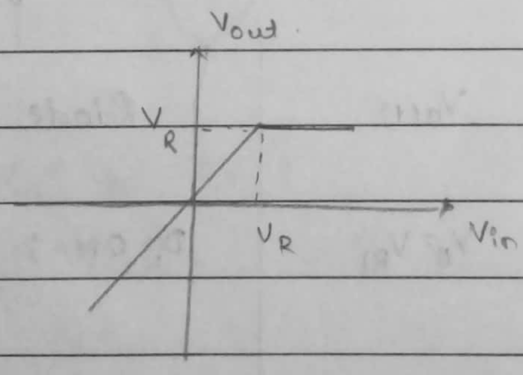


fig 2.a. Circuit diagram.

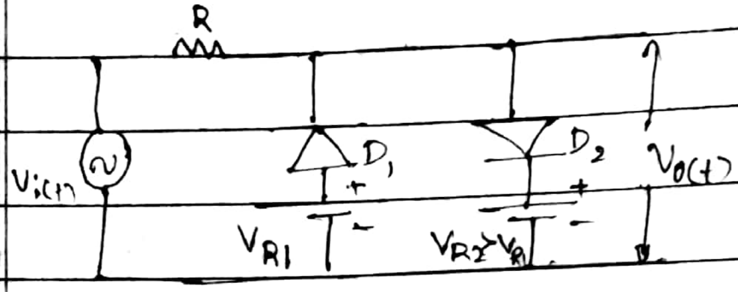


ⓑ waveforms



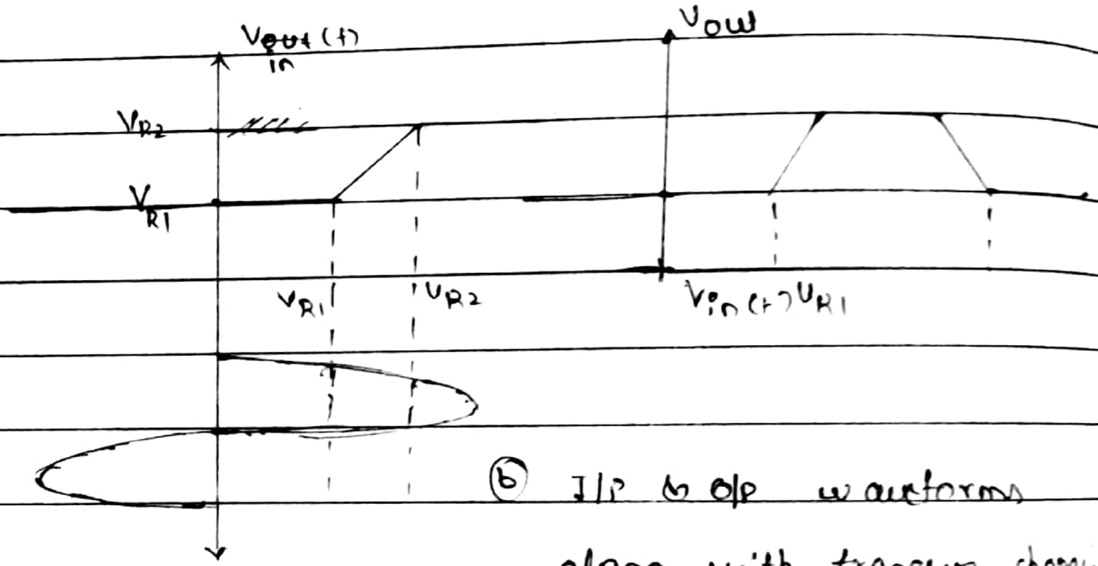
ⓒ transfer char.

imp — Clipping at 2 independent levels. (ideal diodes)



(a) $V_m > V_{R2} > V_{R1}$

$R = \sqrt{R_f \cdot R_r}$



(b) I/P & O/P waveforms along with transfer charac curve

	i/p condition	$V_{o(t)}$	Diode condition
1)	when $V_m < V_{R1}$	$V_0 = V_{R1}$	D_1 = ON ; D_2 = off.
2)	$V_{R1} < V_m < V_{R2}$	$V_0 = V_{m(t)}$	D_1 = off ; D_2 = off
3)	$V_m > V_{R2}$	$V_0 = V_{R2}$	D_1 = off ; D_2 = ON.

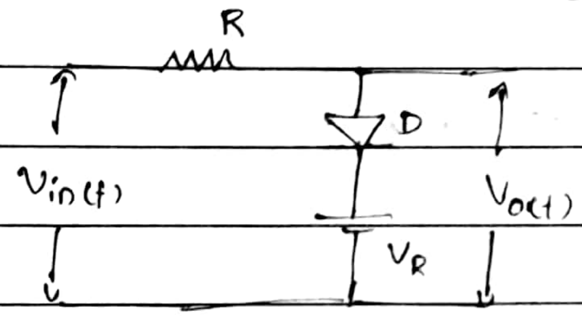
Date : / /
Page No.:

numericals on clipping circuit.

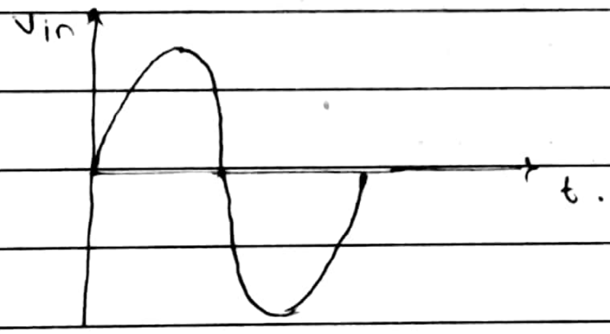
1. For the following diode clipping circuit draw i/p & o/p waveforms for.

a) $R = 100\,\Omega$, b) $R = 1\,k\Omega$ c) $R = 10\,k\Omega$ for v_i -

$v_i = 20 \sin\omega t$, $V_R = 10\,V$, $R_f = 100\,\Omega$, $R_r = \infty$, $V_\gamma = 0\,V$.



$V_m = 20\,V$, $V_R = 10\,V$.

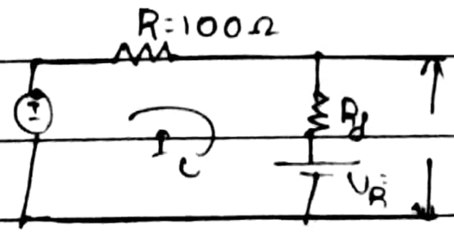


Sol: case i : $V_m < V_R = 10\,V$;

$v_o = v_{i}(t)$.

case ii : $V_m > V_R = 10\,V$; forward biased.

(a)



$$V_o \; I = \frac{V_i(t) - V_R}{R + R_f} \quad \text{—— (1)}$$

$$V_{o(t)} = IR_f + V_R \quad —— ②$$

(a)
$$V_{o(t)} = \left(\frac{V_i - V_R}{R + R_f}\right) \cdot R_f + V_R$$

$$= \left(\frac{20 - 10}{200}\right) 100 + 10$$

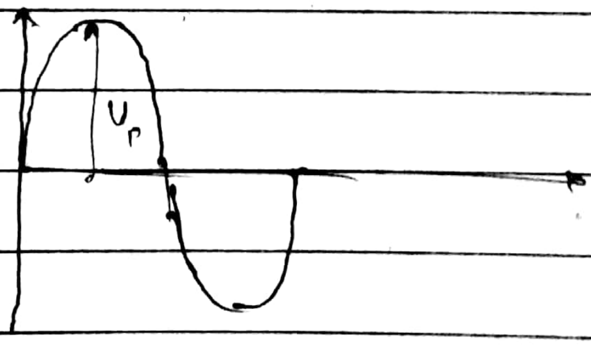
$$\boxed{V_{o(t)a} = 15V}$$

(b)
$$V_{o(t)} = \frac{(20-10)}{1100} \times 100 + 10$$

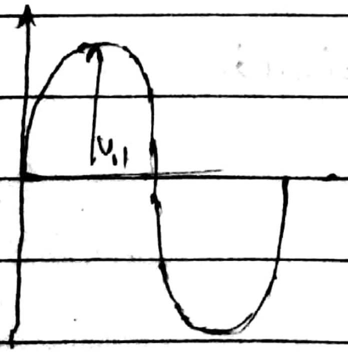
$$\boxed{= 10.9V}$$

(c)
$$V_{o(t)} = \frac{20-10}{(10000+100)} \times 100 + 10$$

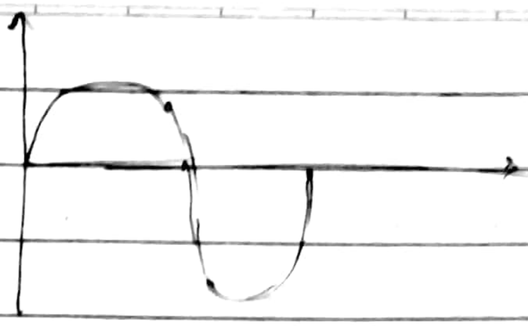
$$\boxed{= 10.099V.}$$



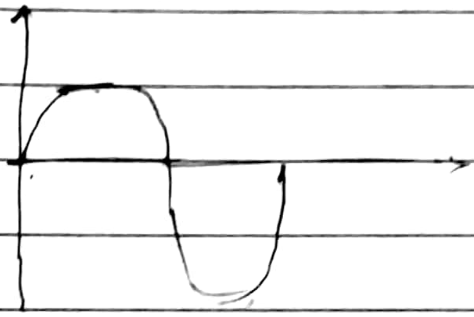
(a)



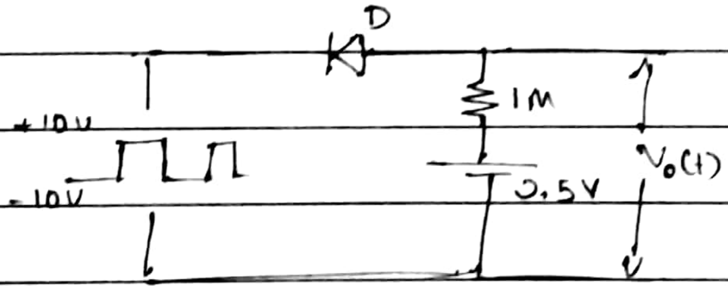
(b)



(c)

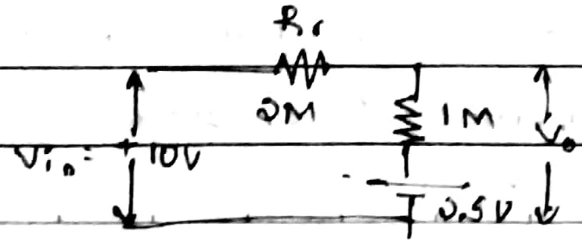


2. Sketch the steady state o/p waveform for the foll'o. circuit indicating max., min., and constant Quotients assume $R_r = 2M\Omega$; $R_f = 0$; $V_r = 0$. i/p is 5kHz square wave varying betn. +10V to ~~-10V~~ -10V.



Sol. when $V_{in(t)} = +10V$; D is reverse biased and it's resistance $R_r = 2M\Omega$.

∴ The equivalent circuit is



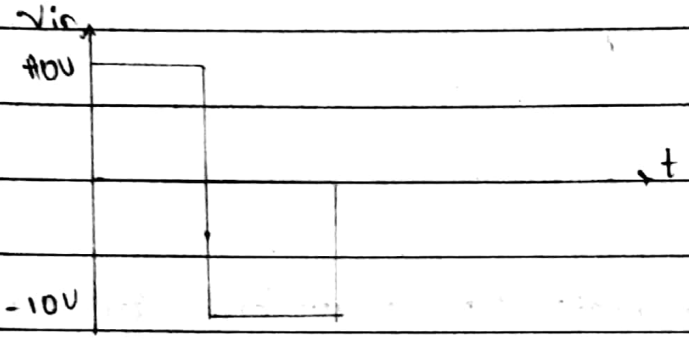
$$I = \frac{V_{in} - V_B}{R_n + R} = \frac{10 - 2.5}{3M}$$

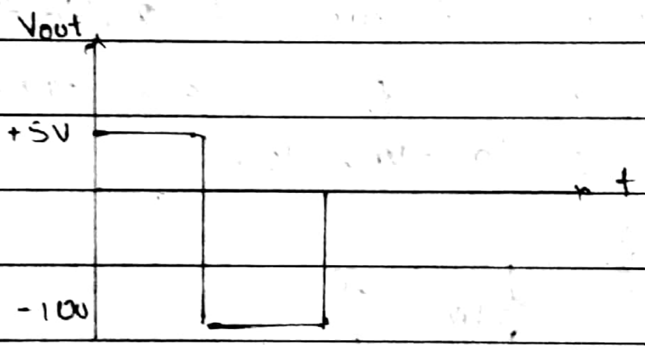
$$= 2.5 \mu A.$$

o/p vol. $V_o = IR$

$$= \cancel{2.5 \mu A (2.5 \times 1 \times 10^6 \times 10^{-6})} + 2.5$$

$$= \cancel{2.5 V} \quad 5V$$





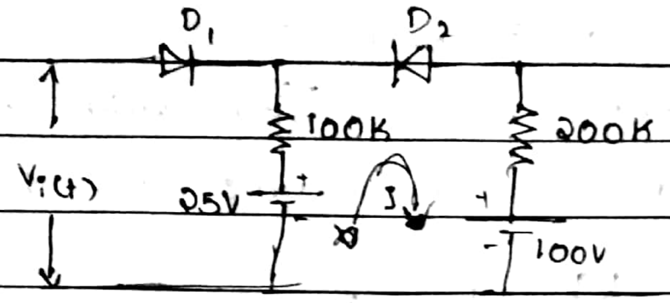
(b) when $V_{in} = -10V$.

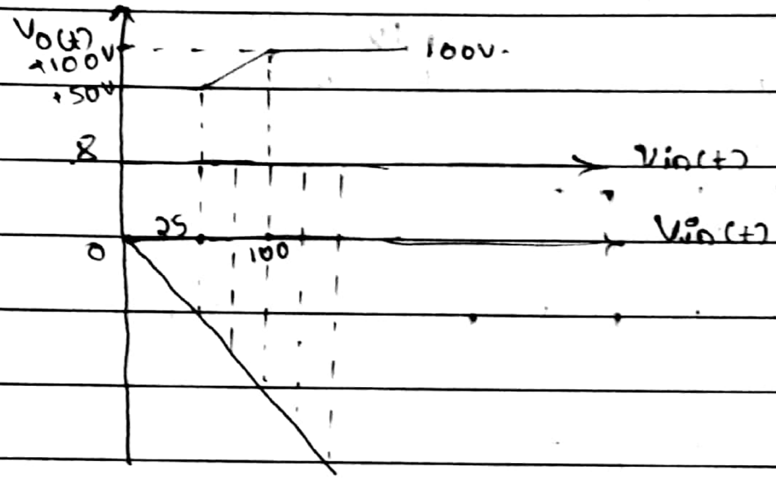
'D' is for. biased ; It's circuits are short

$\therefore V_o = V_{in} = -10V$

3. Sketch the o/p volt. waveform over the i/p volt. for the circuit shown below given that the i/p varies linearly from 0 to 150 V. assume ideal diodes.

Date : / /
Page No.:





Soln:

(i) $I = \dfrac{-100+25}{(200+100)10^3}$ when $V_{in} < 25V$.

$\boxed{I = -0.25\,mA}$

$V_o = I(200 \times 10^3) + 100$

$= -50 + 100$

$= 50V$ //

(ii) when $V_{in} > 25V$, $V_{in} < 100V$, D_1 & D_2 are forward bias.

$\boxed{V_{o(t)} = V_{in(t)}}$

(iii) when $V_{in} > 100V$ //

D_1 is on, D_2 is off.

$\boxed{\therefore V_{o(t)} = 100V}$

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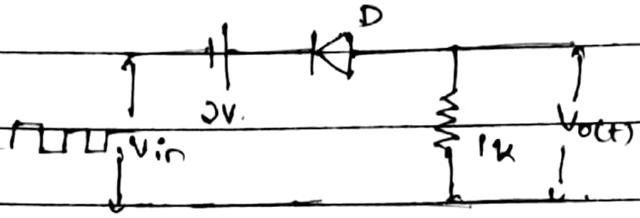
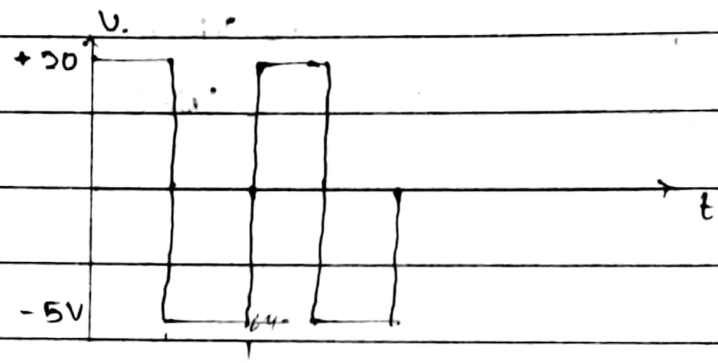
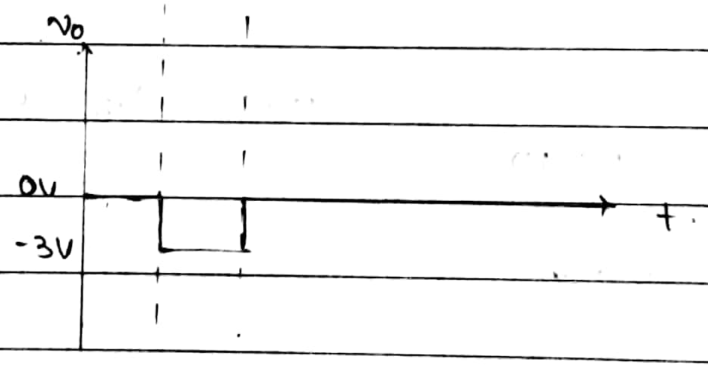
Date : / /
Page No.:

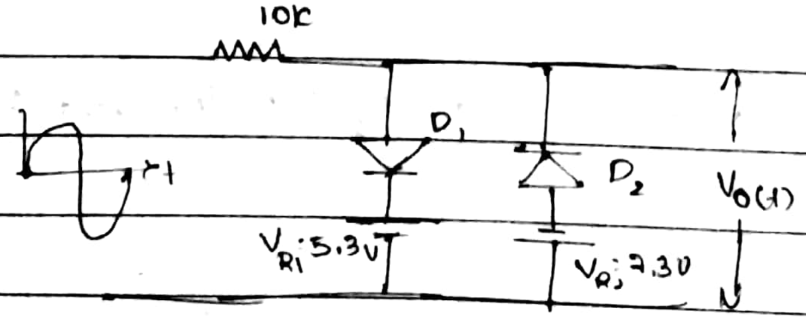
4). The i/p to the follo. circuit is square wave making excursion betn +20V & ~~-20V~~ -5 with equal +ve & -ve intervals plot o/p waveform assume ideal diode.







5). Draw the o/p waveform for the follo. circuit assume $R_f = 0$, $R_r = \infty$, $V_r = 0.7V$



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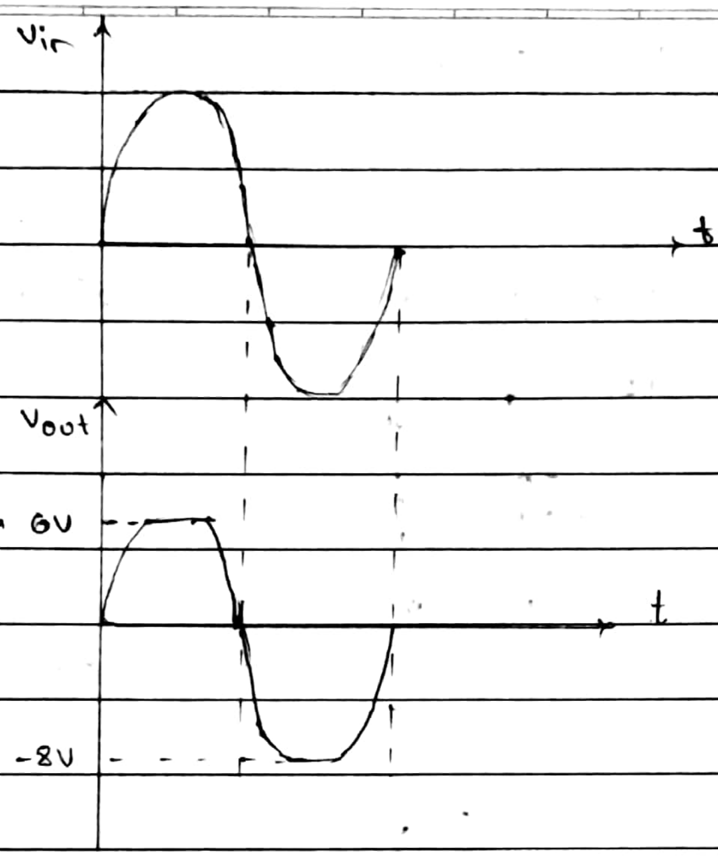
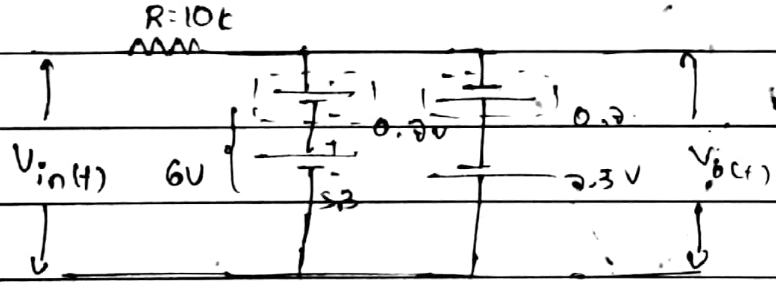
Date : / /
Page No.:



sol^n: Eq circuit.



when $v_{in} \geq 6V$.

D₁ is forward biased.

when $v_{in} \geq -8V$

D_2 is forward biased

23/08/17

for dc - $T(\text{time}) = \infty$

$f = \frac{1}{T} = 0$

$X_c = \frac{1}{2\pi f C} = \infty$ open circuit.

Clamping circuits - (DC restorer or DC - Insertion)

Unbiased :

1) Positive clamping circuit [Ideal diode].

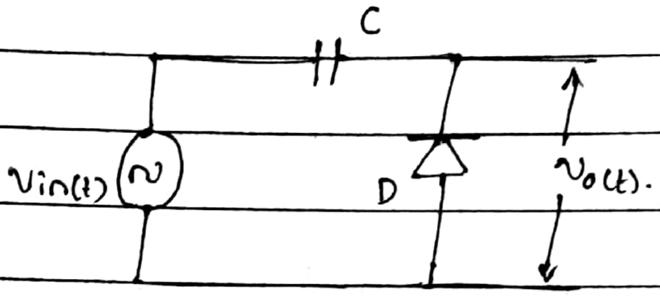


Fig 1 ⓐ circuit diagram

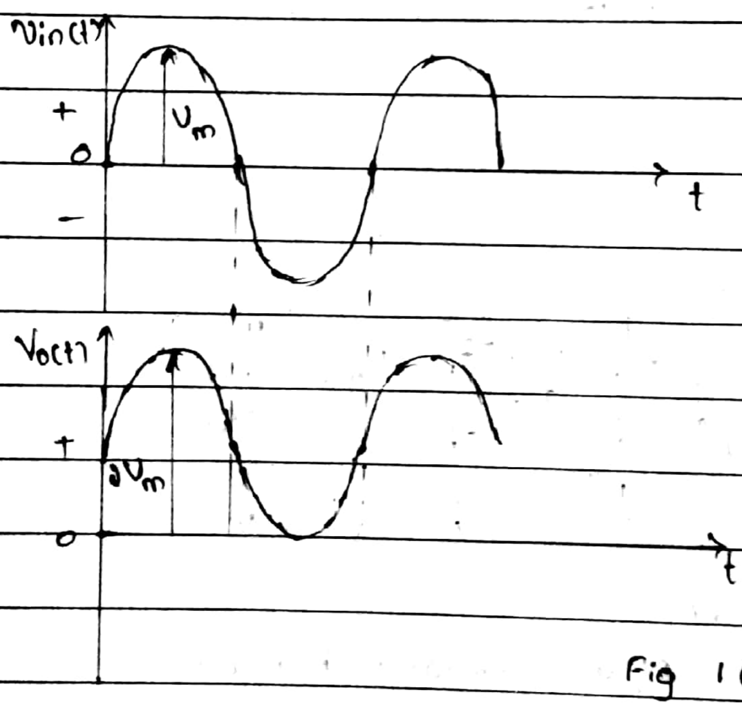
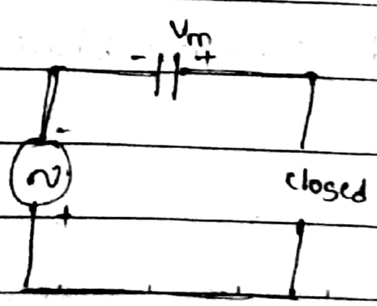
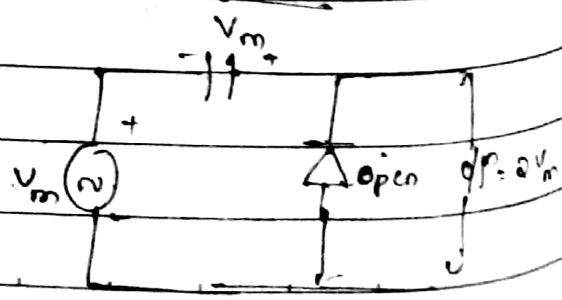


Fig 1 ⓑ waveforms.

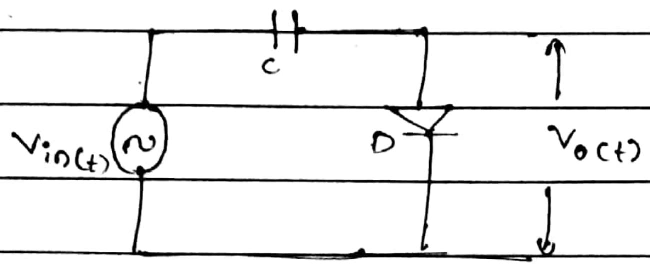
during -ve half cycle:



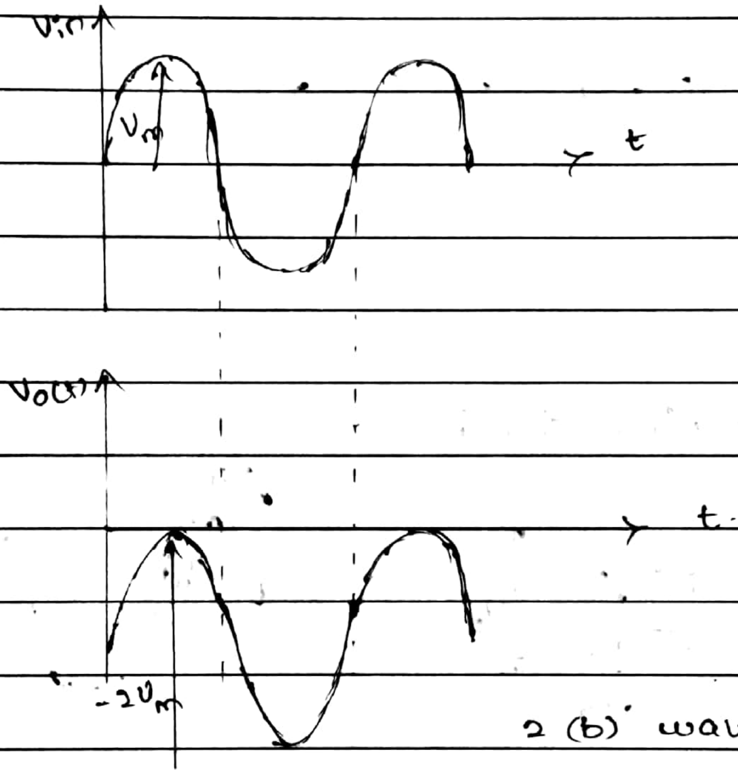
during +ve



2. Negative Clamping Circuit

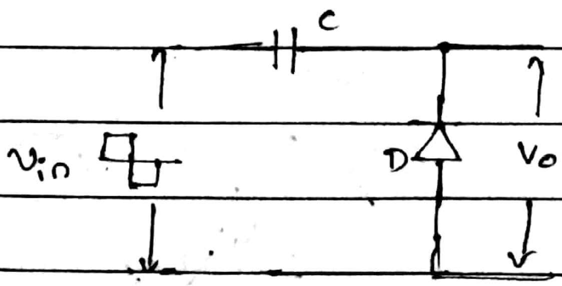


2a : circuit diagram

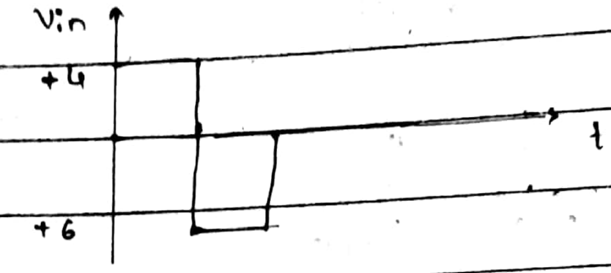


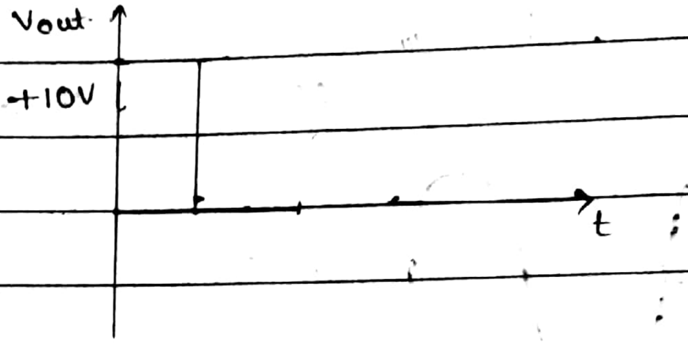
2 (b) waveform.

Ex. for square wave form:



Date: / /
Page No.:

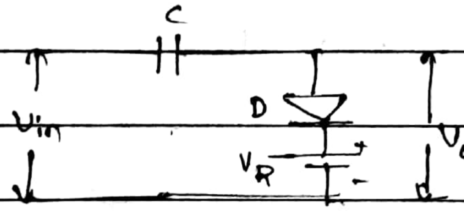


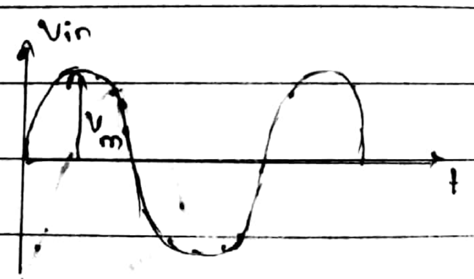


~~Determine~~

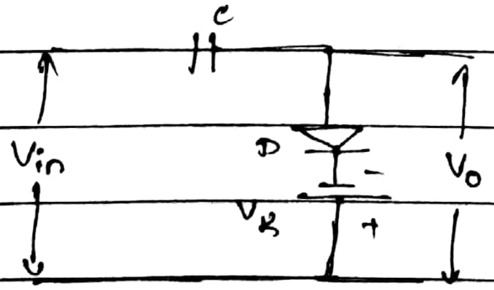
Biased clamping circuit

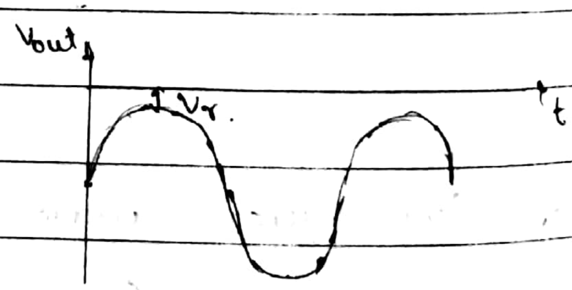
1.





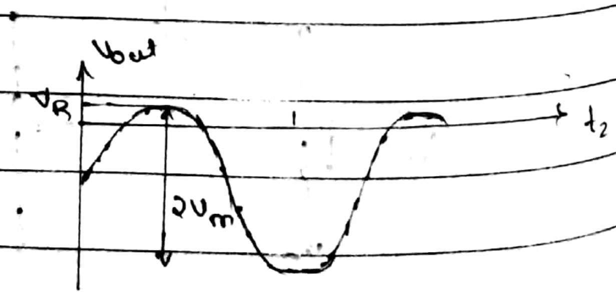
3.1a





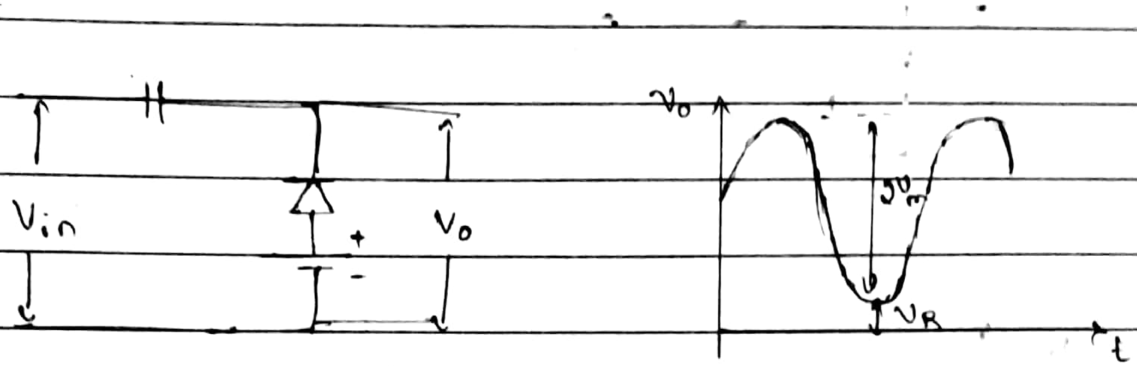
3.1b

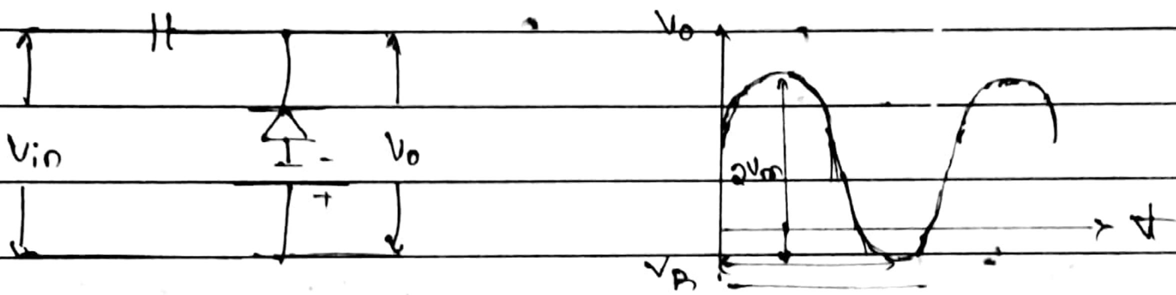
(negative)



Date : / /
Page No.:

2) Positive clamping circuit.





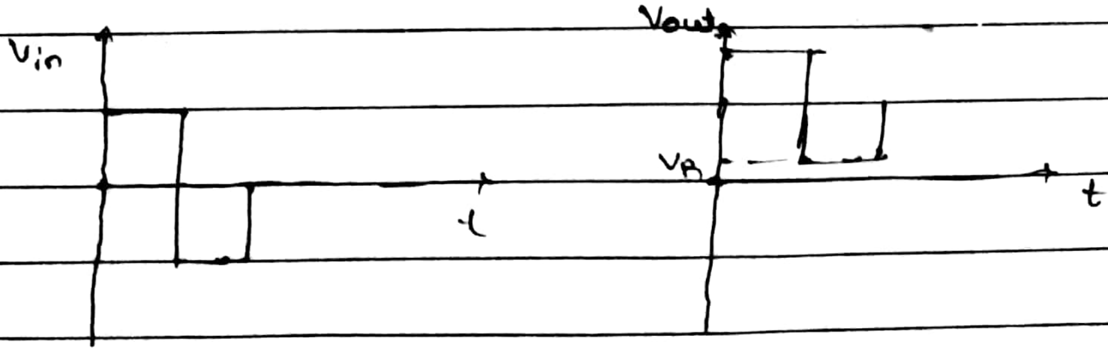
Home work:

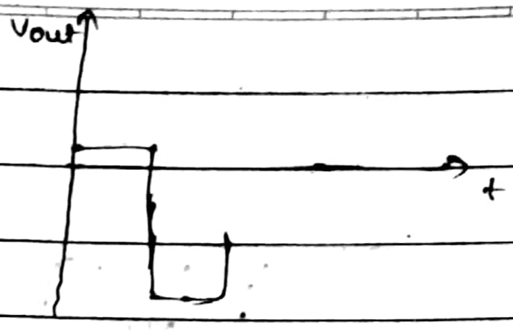
consider square wave as the i/p and draw the circuits.

H.W

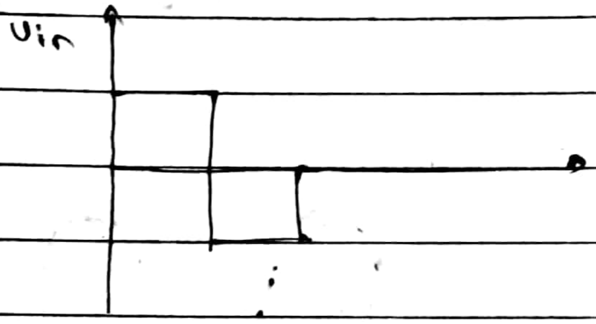
1). Biased clamping circuit.

(i) Positive

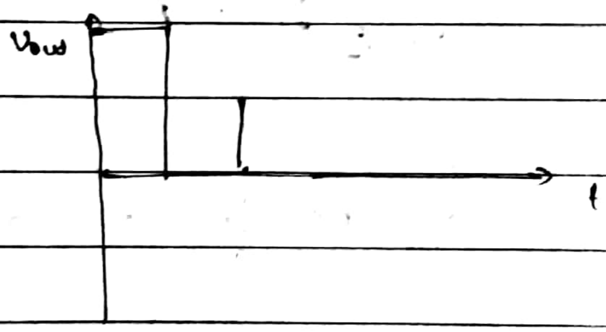




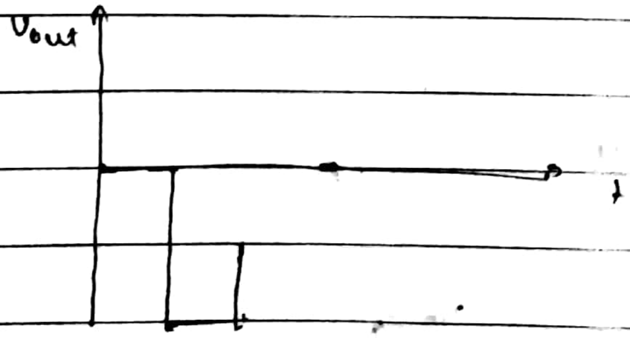
(negative)



(unbiased)



positive clamping



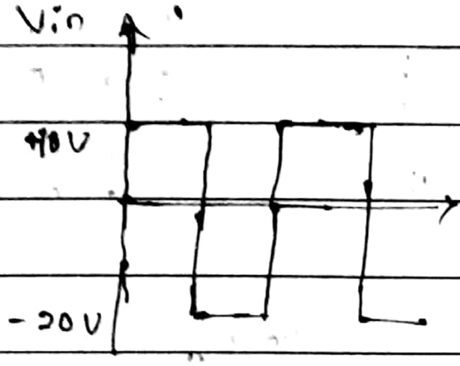
negative clamping.

c/c : closed circuit
o/c : open

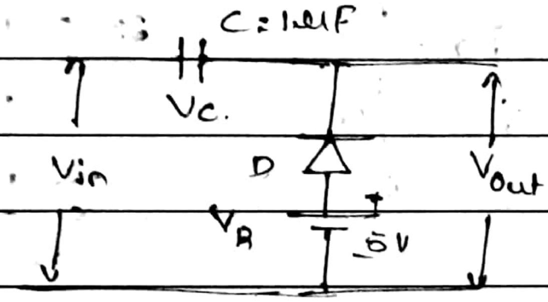
Date : / /
Page No.:

Problems.

1) Determine V_o for the following circuit

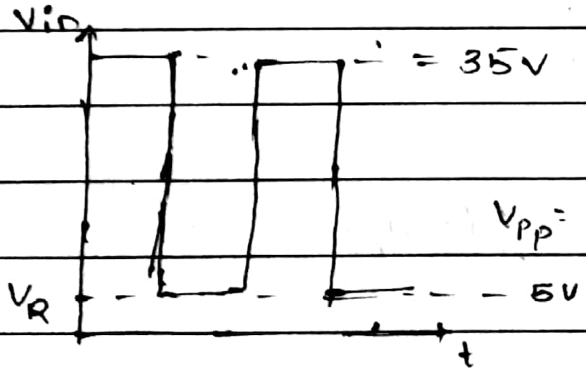


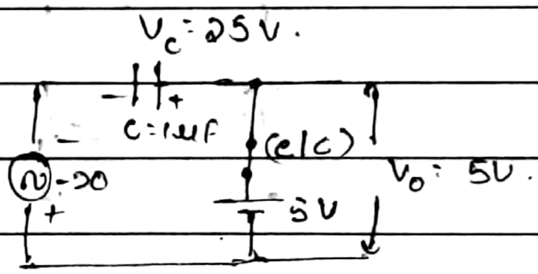
case i)



Soln. during -ve half cycle.

$V_{in(t)} = -20V.$



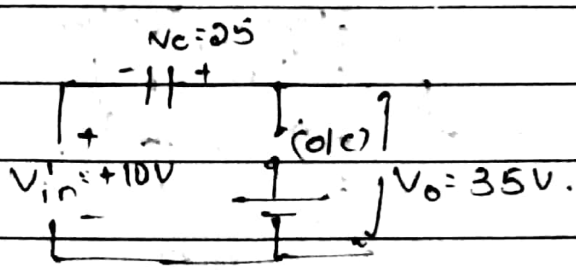


$V_{pp} = 35 - 5 = 30V$

~~$V_o = V_{in}$~~

$V_c = V_{in} + V_{R0}.$

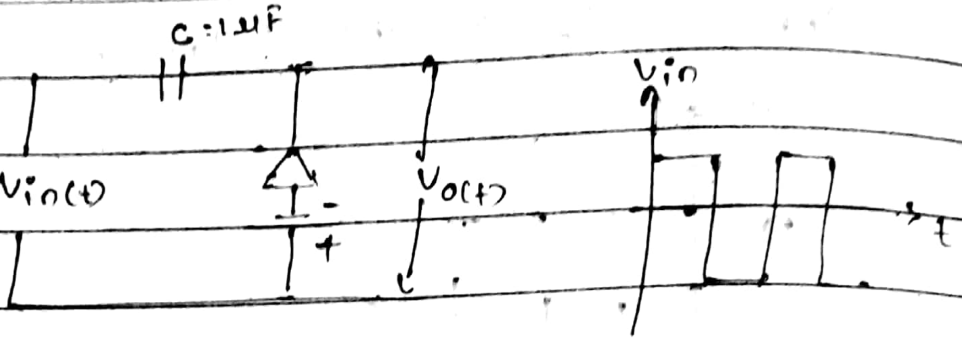
during +ve half cycle.



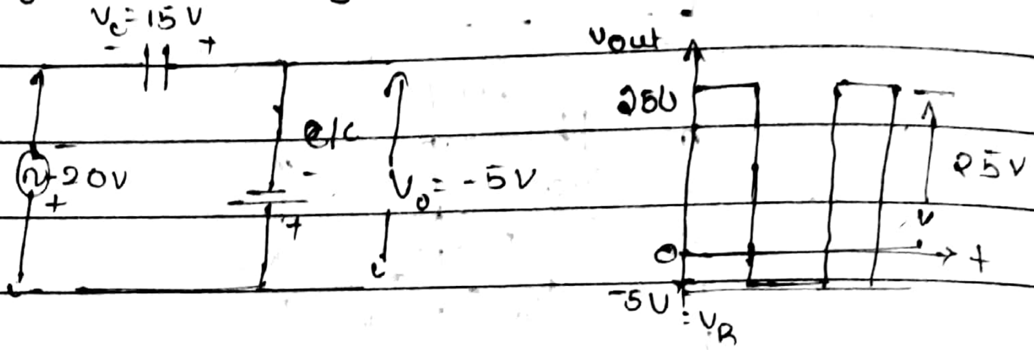
$V_o = V_{in} + V_c = 35$

Date: / /
Page No.:

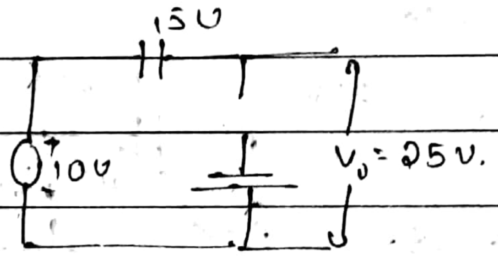
case ii)



during negative half cycle

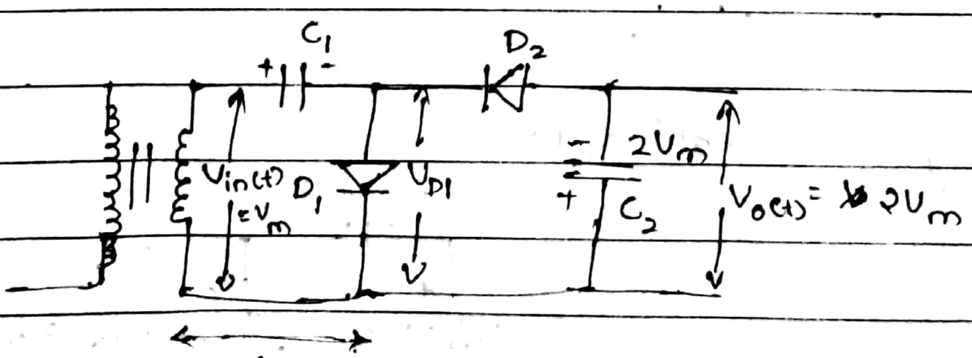


during +ve half cycle.



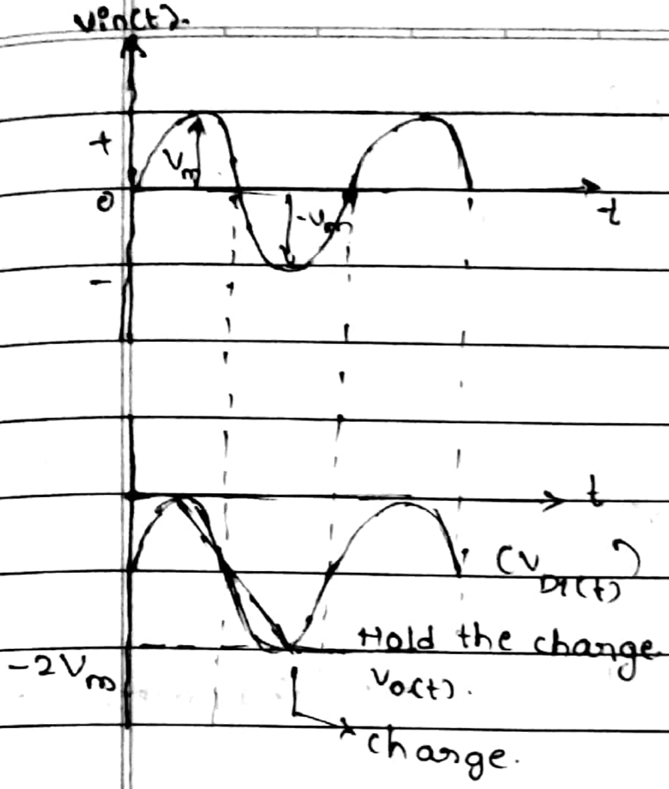
Voltage Doubler using Diodes.

(A)

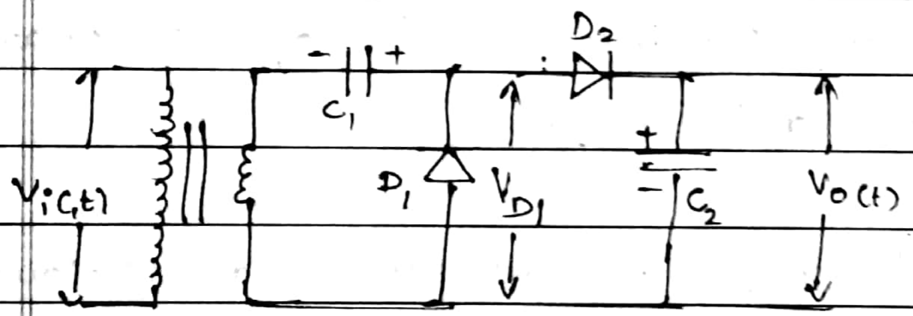


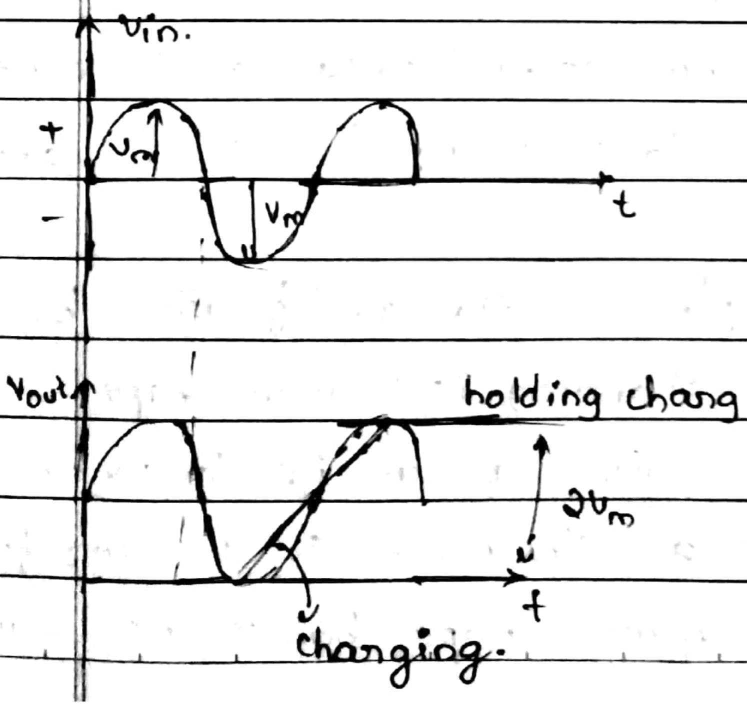
-ve
clamper.

Note: when $V_{in} = V_m$, $V_{out} = -2V_m$.



B) when $V_{in} = V_m$, $V_0 = 2V_m$.





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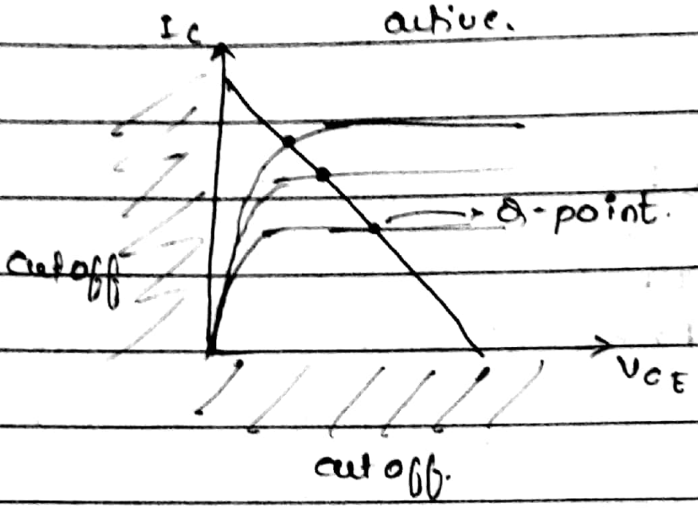
Date : / /

Page No.:

Chapter 02 BJT Applications

Biasing → Q-point → loadline



o/p characteristics

Biasing is required to turn on the device so that it operates in the linear region of it's charac. it is called as active region.

Q-point or op.r.-pt. is intersection of dc-load line in the o/p char. curve

This Q-point has to be located at the centre of active region so that faithful amplification is obtained

Faithful ampl. is the amplification by an active device without changing it's wave shape.
ie if sine wave is given as an i/p for the ampl. o/p should also be a sine wave in an amplified form ie the o/p wave shape has to be same as

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the i/p.

Biasing techniques [CE-configuration].

1. Fixed biasing or Base resistor method.
2. Emmitter resistor method.
3. collector to base feedbak resistor method
4. voltage divider biasing techniques (Universal biasing technique).

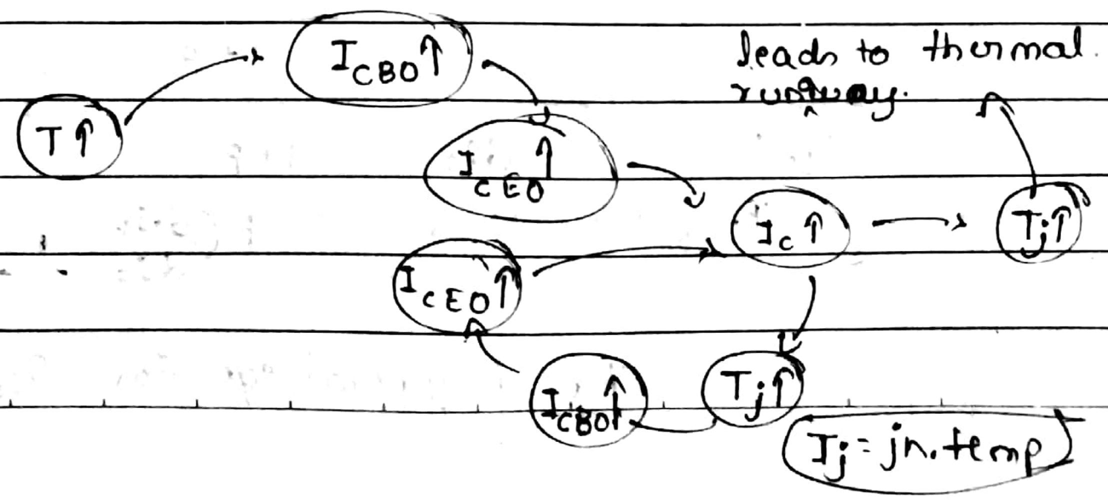
$$I_C = \beta I_B + (1+\beta) I_{CBO} \quad \text{--- (1)}$$

$I_{CBO} = I_{CO} =$ collector leakage current.

$$I_{CE(O)} = (1+\beta) I_{CBO} \quad \text{--- (2)}$$

★ Sequence of events occuring in a transistor which leads to thermal run away.

Thermal runaway is self destruction of an unstablised transistor when there is an increase in the temp.



Note: To avoid thermal runaway. diff. types of biasing are used.

Date : / /
Page No.:

Derivation of General eqn for stability factor (S_{ICO})

$$S_{ICO}\Big|_{V_{BE},\ \beta = \text{costant}} = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$$

$$S_{\beta}\Big|_{V_{BE},\ I_{CO} = \text{const}} = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$$

$$S_{V_{BE}}\Big|_{I_{CO},\ \beta = \text{const}} = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$$

w.k.t. $I_C = \beta \cdot I_B + (1+\beta) I_{CO}$ —— ①

differentating above eqn w.r.t. I_C

$$\frac{dI_C}{dI_C} = \beta \frac{d \cdot I_B}{dI_C} + (1+\beta) \frac{dI_{CO}}{dI_C} \quad \text{—— ②}$$

$$\frac{dI_{CO}}{dI_C} = \frac{1-\beta\left(\frac{d \cdot I_B}{dI_C}\right)}{1+\beta} \quad \text{—— ③}$$

$$\boxed{S_{ICO}\Big|_{\beta \cdot V_{BE} = \text{const}} = \frac{dI_C}{dI_{CO}} = \frac{1+\beta}{1-\beta\left(\frac{d \cdot I_B}{dI_C}\right)}} \quad \text{—— (A)}$$

This is general eqn for S_{ICO}.

Date : / /
Page No.:

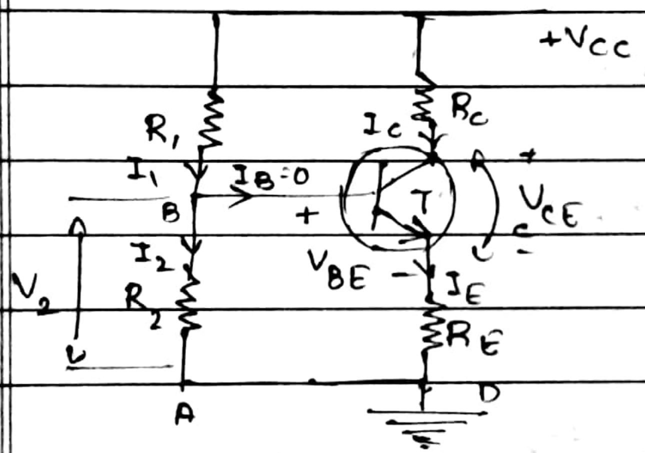
Voltage divider Biasing technique

1.) Using approx. method. {Here, usually β = unknown}.

2.) Using accurate methode

1) Using approximate method :

Analysis ~~using~~



Analysis : here, Base curr. I_B is neglected for simplicity

so that $I_E \doteq I_C$ — ①

looking at the cir. diagram we can say that

$I_1 = I_2$ ($\because I_B = 0$). — ②

$\therefore I_1 = \frac{V_{CC}}{R_1 + R_2}$ — ③

$\therefore V_2 = I_1 R_2$ or $I_2 R_2$

$$\therefore \boxed{V_2 = \frac{V_{CC}(R_2)}{R_1 + R_2}}$$

Q- point
Q - Quisent - silent

Date : / /
Page No.:

Applying KVL to ABCDA.

$$V_2 = V_{BE} + I_E R_E$$

$$= V_{BE} + I_c R_E$$

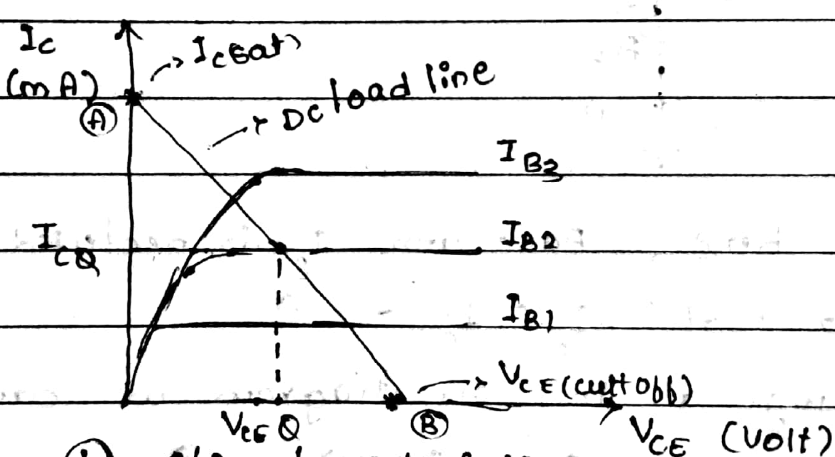
$$\boxed{I_c = \frac{V_2 - V_{BE}}{R_E}} \quad \text{--- (7)}$$

applying KVL to o/p loop.

$$V_{CC} = I_c R_c + V_{CE} + I_E R_E \quad \text{--- (8)}$$

soln $I_E = I_c$

$$V_{CC} = I_c (R_c + R_E) + V_{CE} \quad \text{--- (9)}$$



(b) o/p characteristics

consider eqn '9' and let us put $V_{CE} = 0$

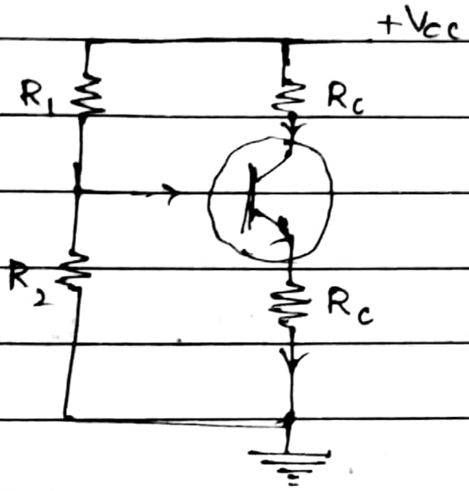
$$I_c = \frac{V_{CC}}{(R_c + R_E)} \quad \text{--- pt (A)}$$

let $I_c = 0$

$$V_{CE} = V_{CC} \quad \text{--- pt (B)}$$
(cutoff)

DC load line

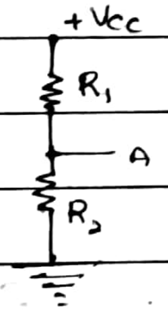
2) Analysis using accurate methode



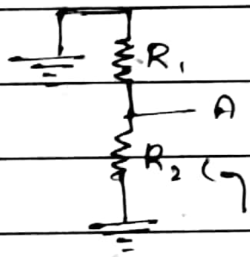
$I_c + I_B = I_E$

Fig 2.a

$I_B = 0.$

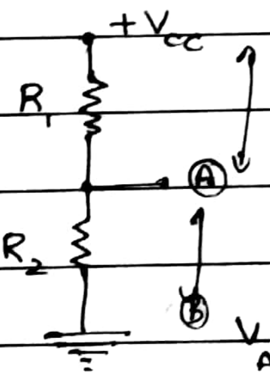


(b)



$R_{Th} = R_1 \| R_2$

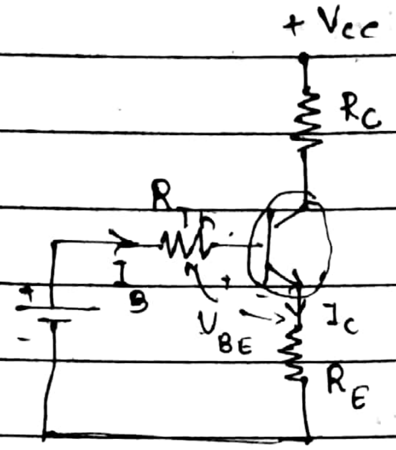
(c)



$V_{AB} = V_{o/p} = V_{Th} = \dfrac{V_{cc} * R_2}{R_1 + R_2}$

(d)

Date : / /
Page No.:



(e) Theivinen's equivalent ckt. to the i/p. section

Analysis: Apply. KVL to the i/p loop.

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

Sub: $I_E = (1+\beta) I_B$

$$\boxed{I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E}} \quad \text{—— (A)}$$

$$\boxed{I_c = \beta I_B}$$

Apply. KVL to. o/p loop

$$\therefore V_{cc} = I_c R_c + V_{CE} + I_E R_E \quad \text{—— (4)}$$

neglecting I_B, $I_E \simeq I_c$

$$V_{cc} = I_c R_c + V_{CE} + I_E R_E \quad \text{—— (5)}$$

$$I_c = \frac{V_{cc} - V_{CE}}{R_c + R_E} \qquad V_{CE} = V_{cc} - I_c (R_c + R_E) \quad \text{—— (6)}$$

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Date : / /
Page No.:

$\therefore$ Qpt (V_{CEQ}, I_{CQ}).

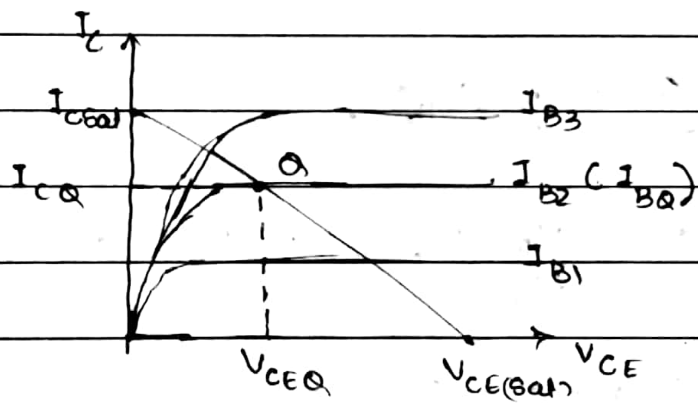
considering Eqn (6) i.e $V_{CC} = I_C(R_C + R_E) + V_{CE}$ — (7)

we can draw dc-load line by putting $I_C = 0$ in the upper eqn.

$$V_{CE_{cutoff}} = V_{CC} \longrightarrow pt\,(A).$$

put $V_{CE} = 0$.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \longrightarrow pt\ (B)$$



DC load line.

<u>Derivation of S_{Ico} for this biasing ckt.</u>

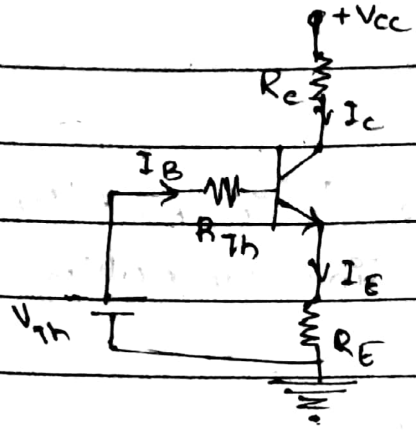
we know that,

$$S_{Ico}/_{\beta \cdot V_{BE} = const} = \frac{1+\beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)} \longrightarrow (A)$$

$$S_{I_{co}} = \frac{dI_c}{dI_{co}}$$

Date : / /

Page No.:



$$V_{Th} = \frac{V_{cc} \cdot R_2}{R_1 + R_2}$$

$$\therefore \quad V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E \quad \text{—— (i)}$$

$$\text{Sub} \approx I_E = I_c + I_B$$

$$V_{Th} = I_B (R_{Th} + R_E) + I_c R_E + V_{BE} \quad \text{—— (ii)}$$

$$\frac{dV_{Th}}{dI_c} = \frac{dI_B}{dI_c}(R_{Th} + R_E) + \frac{dI_c}{dI_c} \cdot R_E + \frac{dV_{BE}}{dI_c}$$

$$\cancel{\frac{dV_{Th}}{dI_c} = \beta (R_{Th} + R_E)}$$

$$0 = \frac{dI_B}{dI_c}(R_{Th} + R_E) + \cdot R_E + 0$$

$$\therefore \frac{dI_B}{dI_c} = \frac{-R_E}{(R_E + R_{Th})} \quad \text{—— (iii)}$$

Subsbituting (iii) in (A)

$$\underset{V_{BE} \, \& \, \beta \text{ const}}{S_{I_{co}}} = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_{Th}}\right)}$$

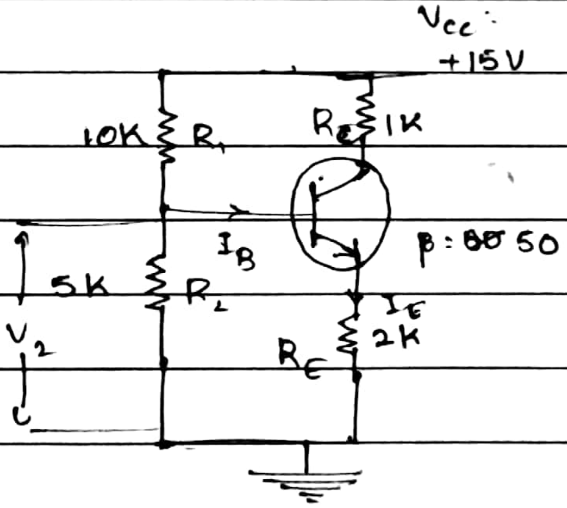
In the above equation, if $R_{Th} << R_E$

then $S_{I_{co}} = \frac{1+\beta}{1+\beta} = 1$ //

To stabalise the operating point it is req. to keep the collector current variation as small as possible whenever there is leakage in .

Hence, stability factor what we obtained in this voltage biasing method is much better than any other biasing technique hence it is called as universal biasing method.

1) draw the dc load line and locate op-point for the following voltage divider biasing ckt. using approximate method as well as accurate method. transistor used is of Si type.



(a) approximate methode,

$$I_1 = \frac{V_{cc}}{R_1 + R_2} = \frac{15}{10k + 5k} = 1mA$$

$$V_2 = I_1 \cdot R_2 = 1 \times 10^{-3} \times 5 \times 10^{3}$$

$$= 5V$$

Date: / /
Page No.:

$V_2 = I_E R_E + V_{BE} = V_{BE} + I_C R_E$

$I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{2k} = \frac{4.3}{2k}$

$\boxed{I_{C_Q} = 2.15 \text{ mA}}$ //

o/p loop:

$V_{CC} = I_C(R_C + R_E) + V_{CE}$

$V_{CE} = 15 \cancel{15} - (2.15(10^{-3})(2+1)\times 10^3)$

$= \cancel{10.7}\ 15 - 6.45$

$\boxed{V_{CE_Q} = 8.55 \text{ V}}$ //

$V_{CC} = I_C(R_C + R_C) + V_{CE}$

put $I_C = 0$.

$\boxed{V_{CC} = V_{CE_{cutoff}} = 15 \text{ V}.}$ — (A)

put $V_{CE} = 0$

$I_{C_{sat}} = \frac{15}{(2+3)\times 10^3}$

$\boxed{I_{C_{sat}} = 5 \text{mA}}$ — (B)

∴ Q pt values ⇒ $V_{CEQ} = 8.55\text{V}$, $I_{CQ} = 2.15\text{mA}$ //

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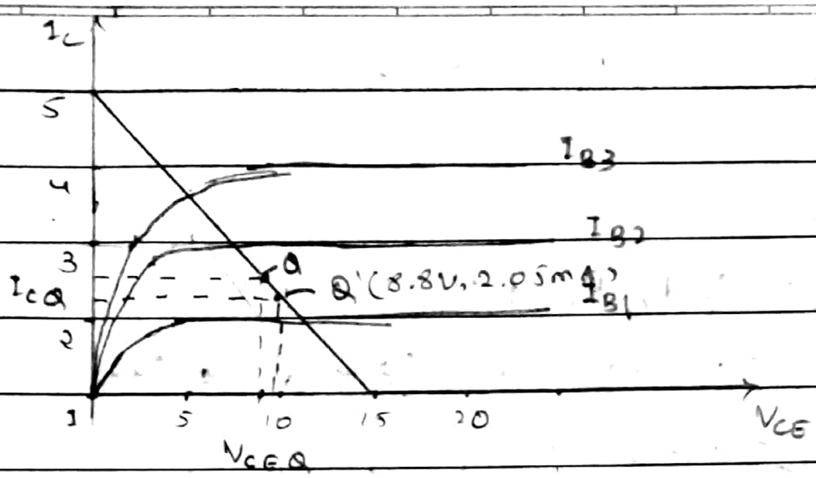
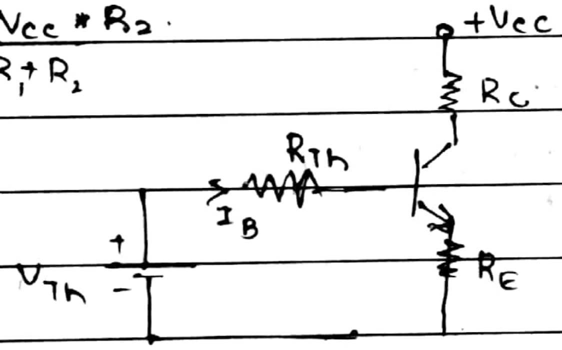
Date : / /
Page No.:



b) <u>using accurate methode.</u>

$V_{Th} = \dfrac{V_{cc} * R_2}{R_1 + R_2}$



$V_{Th} = \dfrac{15}{15 \times 10^3} \times 5 \times 10^3$

$= 5V$ //

$\dfrac{R_1}{R_2} = \dfrac{10}{5} = \cancel{2}$

$R_1 \| R_2 = \dfrac{10 \times 5}{15} = 3.33k\Omega$

$= \dfrac{R_1 \times R_2}{R_1 + R_2}$

$V_{Th} = I_B R_{Th} + V_{BE} + R_E I_E$

$V_{Th} = I_B R_{Th} + V_{BE} + (1+\beta) I_B \cdot R_E$

$I_{BQ} = \dfrac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E}$

$= \dfrac{5 - 0.7}{(3.3 + (51)2) 10^3}$

$= \cancel{408}$ $40.8\ \mu A$ //

Date : / /
Page No.:

$I_{C_Q} = \beta I_B = 50 \times 40.8 \mu A = 2.05 mA$ //

o/p loop

$V_{CE} = I_C(R_C + R_E) + V_{CE}$ — ⑤

$V_{CE} = -(2.05 \times 10^{-3})(3 \times 10^{3}) + (15$

$V_{CEQ} = 8.85V$ //

V_{CC} = considering ⑤ let us determine dc load line pt.

put ~~$V_{CE} = 0$~~ $I_C = 0$

$V_{CE_{cut}} = V_{CC} = 15 V$

$V_C = 0$

$I_{Csat} = \frac{15}{3 \times 10^{3}} = 5mA.$

Q-point values are $V_{CEQ} = 8.85V$

$I_{CQ} = 2.05mA$

$(8.8V, 2.05mA) = Q'$

$S_{I_{CO}} = \frac{1+50}{1+50\left(\frac{2}{5.3}\right)} = 2.56$

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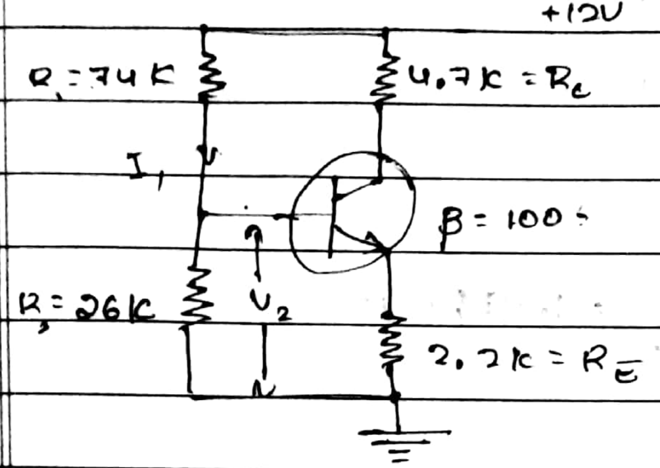
2).



a) approx. method.

$$I_1 = \frac{V_{cc}}{R_1 + R_2} = \frac{12}{(74+26)10^3} = 0.12 \text{ mA}$$

$$V_2 = I_1 R_2 = (0.12 \times 10^{-3})(26 \times 10^3)$$
$$= 3.12 \text{V}$$

$$V_2 = I_E R_E + V_{BE} \qquad (I_C = I_E \because I_B = 0$$
$$= I_C R_E + V_{BE}$$

$$I_C = \frac{3.12 - 0.7}{2.2 \times 10^3}$$

$$I_C = 1.1 \text{ mA}$$

O/P loop.

$$V_{CC} = I_C R_C + I_C R_E + V_{CE}$$

$$V_{CE} = \frac{V_{CC}}{I_C (R_C + R_E)} = \frac{12}{}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 4.41 \text{V}$$

(a)

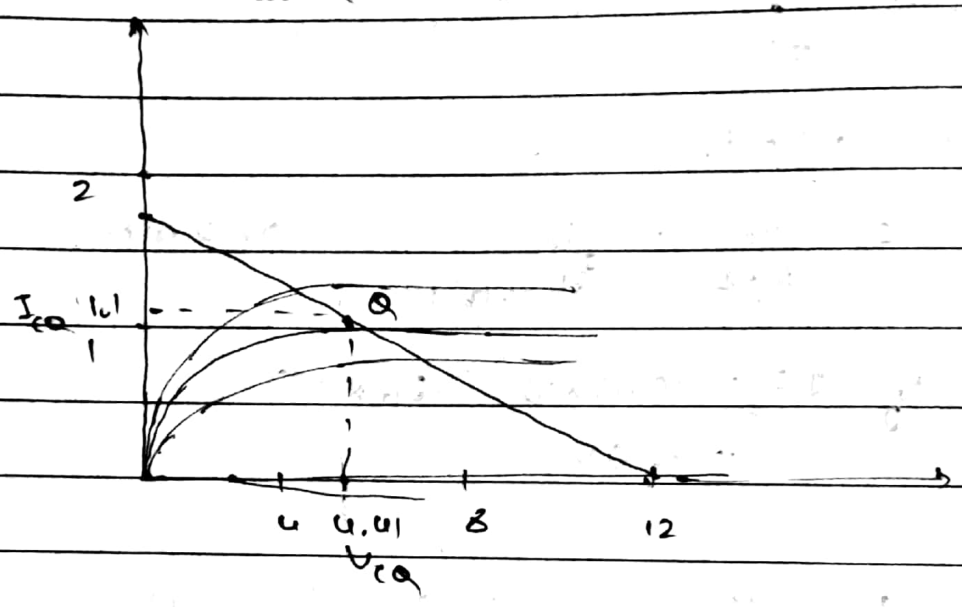
Date : / /
Page No.:

put $V_{cc} = I_C = 0$ in (a)

$\therefore V_{CE_{cutoff}} = V_{cc} = 12V.$

Put $V_{CE} = 0$ in (a)

$$I_{C_{sat}} = \frac{12}{(6.9 \times 10^3)} = 1.739 \text{ mA.}$$



accurate method.

$$V_{TH} = \frac{V_{cc} * R_2}{R_1 + R_2} = \frac{12}{(100 \times 10^3)} \times (26 \times 10^3)$$

$$= 3.12V$$

$$R_{TH} = \frac{R_1 \cdot R_2}{R_1 + R_2} = \cancel{63 \times 26}\ \frac{74 \times 26 \times 10^6}{100 \times 10^3} = 19.24\ k\Omega$$

Date : / /

Page No.:

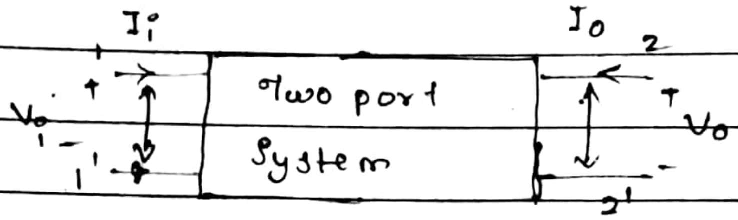
re-model

Transistor modeling <

(BJT ")

hybrid model.

Hybrid parameters & hybrid Equation model for BJT



$V_i = h_{11} I_i + h_{12} V_o$

$I_o = h_{21} I_i + h_{22} V_o$

here i/p current I_i and o/p volt. V_o are consider as independent variablo whereas i/p V_i and o/p current I_o are consider as dependent variables

as h_{11} to h_{12}, h_{21}, h_{22} are called as ~~hyd.~~ hybrid parameters or h-parameter.

* $h_{11}\Big|_{V_o=0} = \frac{V_i}{I_i} = h_i$ = short circuit i/p impedence or resistance. => hie (CE-conf)

* $h_{12}\Big|_{I_i=0} = \frac{V_i}{V_o} = h_r$ = open ckt. reverse volt. transfer ratio. => hre (CE-conf.).

~~Z = R + j X.~~

impedance → admitance

reactance → acceptance

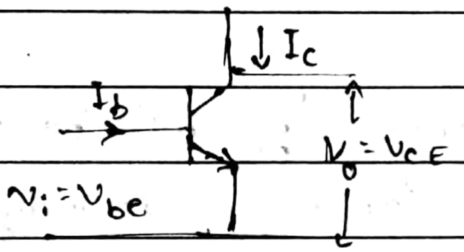
Date : / /

Page No.:

* $h_{21}\Big|_{V_o=0} = \frac{I_o}{V} \frac{I_o}{I_i}$ = short ckt forward current transfer ratio. : $h_f = h_{fe}$ (CE)

* $h_{22}\Big|_{I_i=0} = \frac{I_o}{V_o}$ = open ckt. conductance & admitance : $h_o \Rightarrow h_{oe}$ (CE)

Let us use these hybrid parameters. for BJT in CE configuration.



$I_i = I_b$, $I_o = I_c$

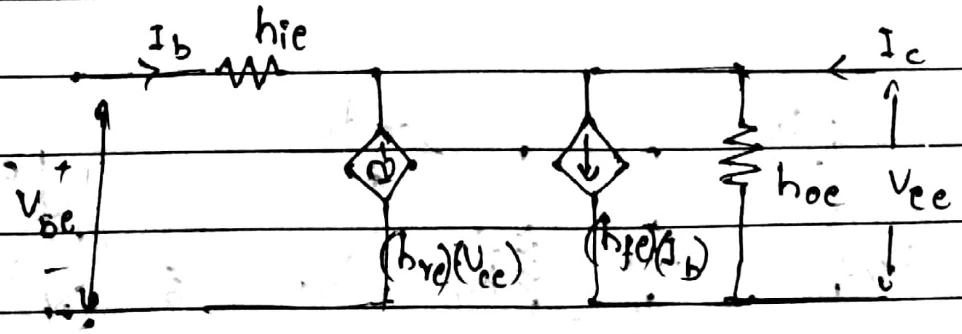
$V_i = V_{be}$

$V_o = V_{cE}$

$V_i = V_{be} = h_{ie} I_b + h_{re} V_{ce}$ —— (a)

$I_o = I_c = h_{fe} I_b + h_{oe} V_{ce}$ —— (b)

considering eqn (a) & (b) let us draw equivilant ckt for BJT which is called as hybrid eq. model



(B) hybrid equivalent model.

04/09/17

Date : / /
Page No.:

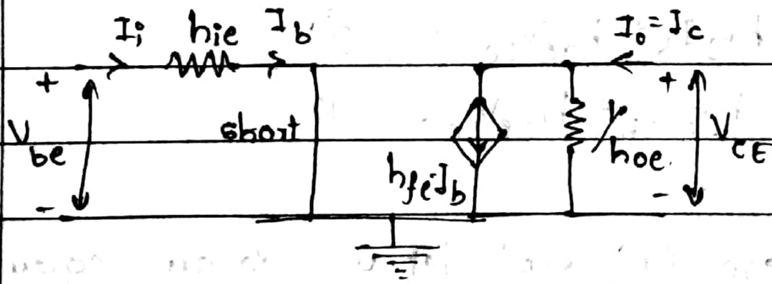
As seen from above hybrid model h_{re} represent reverse volt transferation and this will be neglegeble and hence $(h_{re} \times V_{CE})$ will be neglegeble. ie $\{h_{re} \times V_{CE} \simeq 0\}$.

Then independent source at i/p side can be replaced by short ckt. as shown in fig.

Illy o/p conductance h_{oe} can also be written written as $1/h_{oe}$ by considering it as resistance then we call this circuit as an approx hybrid equivalent model.

Note:

Usually o/p resistance $1/h_{oe}$ will be very large and this will be neglected for some at analysis.



An approx. hybrid equivalent model fig.2

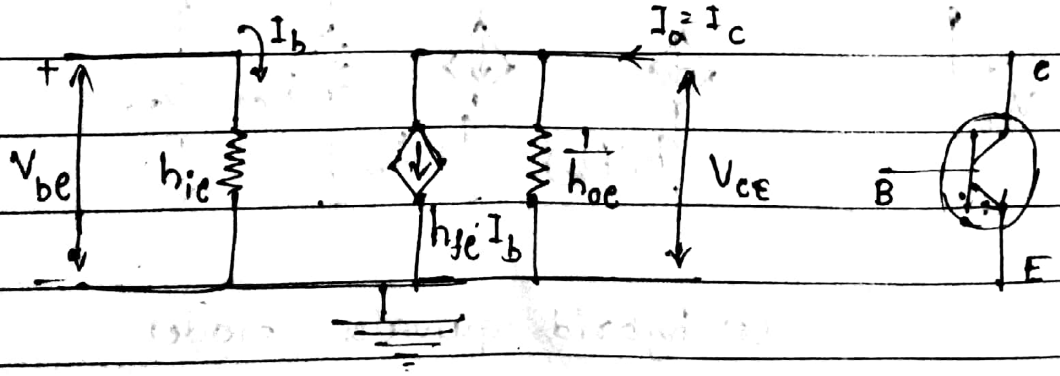


fig 2.b

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Date : / /
Page No.:

Hybrid equivalent model for a voltage divider biasing network. when this is used as an amplification CE conf.

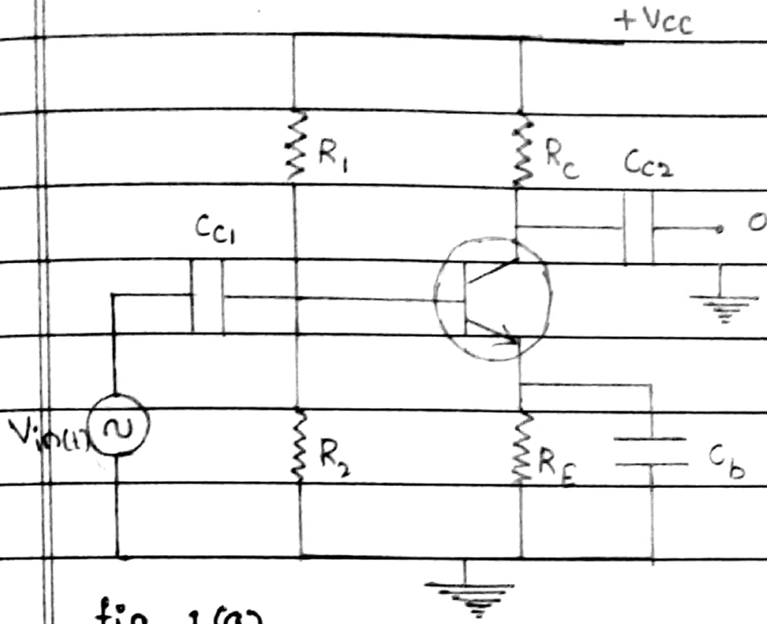


fig 1(a)

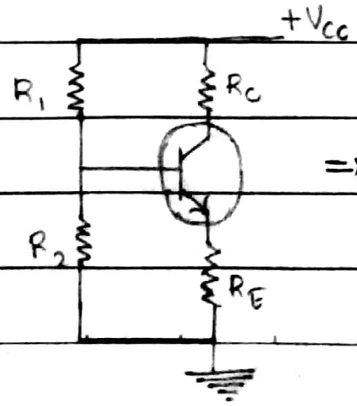
An amplifier ckt. using voltage divider biasing (CE-mode)

*). C_{C1} & C_{C2} => coupling capacitor.

*). C_b => By pass capacitor.

Let us draw Draw equivalent. ckt. for the ckt shown in fig (1a) this is drawn by open circuiting all the capacitors in this ckt.

1b) DC equivalent ckt.



=> (I_{CQ}, V_{CEQ}) & I_{BQ}

(Q.pt values)

Date : / /
Page No.:

Negative sign in the above eqn shows that there is 180° phase difference in i/p & o/p voltages.

4). Current Gain $A_I = \frac{I_o}{I_i}$

where $I_i = \frac{V_i}{Z_i}$ —— (a)

$I_o = V_o / Z_o$ —— (b)

where $Z_i = hie // (R_1 || R_2)$ —— (c)

& $V_i = I_b \cdot hie$ —— (d)

& $Z_o = R_C // (1/hoe)$. —— (e)

$\frac{I_o}{I_i} = \frac{V_o/Z_o}{V_i/Z_i} = \frac{V_o / R_C || (1/hoe)}{V_i / hie || (R_1 || R_2)}$ —— (f)

$\therefore A_I = \frac{I_o Z_o / \cancel{[R_C || (1/hoe)]}}{I_i Z_i / \cancel{[(hie / (R_1 || R_2))]}}$

$A_I = \frac{I_o}{I_i} A_v$

$I_b = \frac{V_i}{hie}$

$I_c = \frac{V_o}{(1/hoe)}$

Date : / /
Page No.:

$$\frac{I_c}{I_b} = \frac{V_o / h_{ie}}{V_i / (1/h_{oe})}$$

$$A_I = A_v \cdot \frac{1}{(h_{ie} \cdot h_{oe})}.$$

$$\therefore \quad A_I = \frac{V_o / R_c \| (1/h_{oe})}{V_i / h_{ie} \| (R_1 \| R_2)}$$

$$= \frac{I_c Z_o / \{R_c \| (1/h_{oe})\}}{I_b \cdot h_{ie} / [(h_{ie} \| (R_1 \| R_2))]}$$

$$= \frac{I_c \cdot (R_c \| 1/h_{oe}) / \{R_c \| (1/h_{oe})\}}{I_b \cdot h_{ie} / [\{h_{ie} \| (R_1 \| R_2)\}]}$$

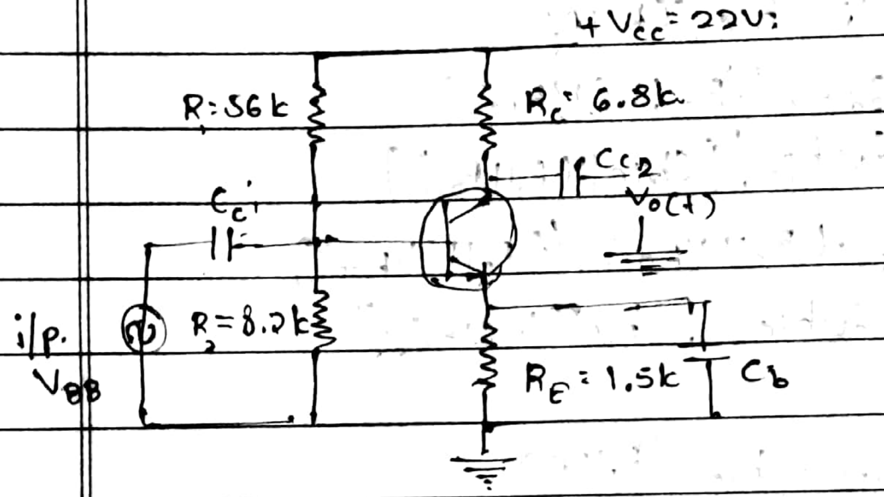
$$= \frac{h_{fe} \times h_{ie} \cdot (R_1 \| R_2)}{h_{ie} (h_{re} + R_1 \| R_2)}$$

$$= \frac{h_{fe} \cdot (R_1 \| R_2)}{(h_{re} + R_1 \| R_2)} \quad //.$$

Date : / /

Page No.:

1) Determine all four parameters of an amplifier using volt. divider ckt. given the $R_1 = 56\,k\Omega$, $R_2 = 8.2k$, $R_C = 6.8k$, $R_E = 1.5k$, $V_{CC} = 22V$. draw the ckt diagram draw it's dc equ. ckt, AC eqv. ckt and corresponding hybrid model.



$h_{fe} = 90$

$h_{ie} = 2k\Omega$

$1/h_{oe} = 50\,k\Omega$

fig 1a.

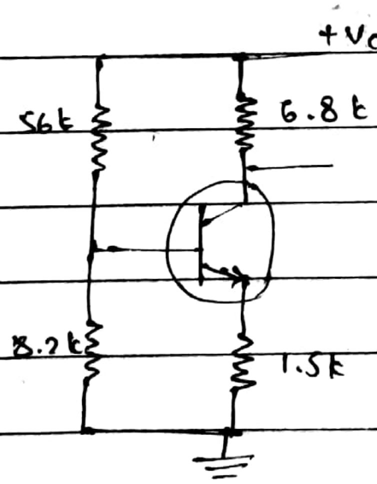


fig 1.b.

(dc equ. model).

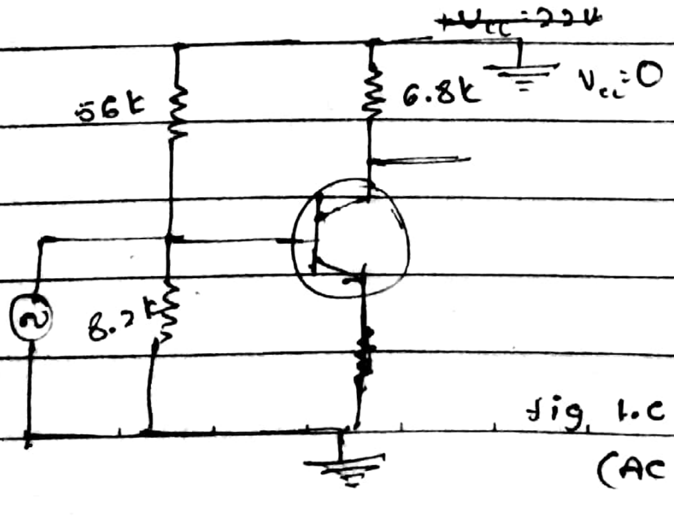
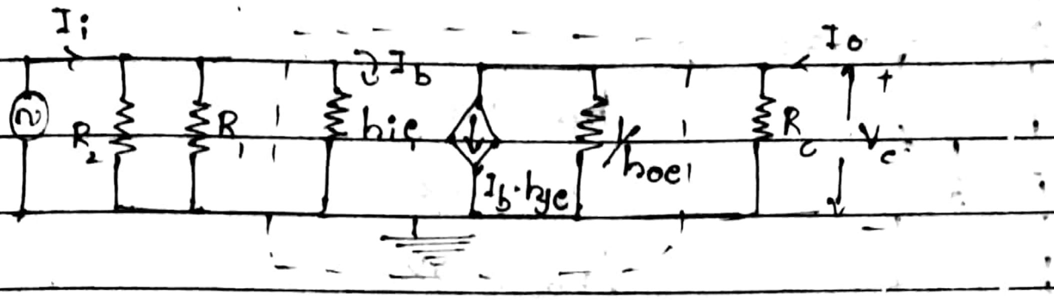


fig. 1.c

(Ac equ. ckt)

hybrid equivalent.



(i) $Z_i = h_{ie} \parallel (R_1 \parallel R_2)$

$= 2000 \parallel (7.153 \times 10^3)$

$= 1562.98\ \Omega$

$\boxed{Z_i = 1.56\ k\Omega}$

ii) $Z_o = R_c \parallel 1/h_{oe} = \dfrac{6.8 \times 50}{(6.8 + 50)}$

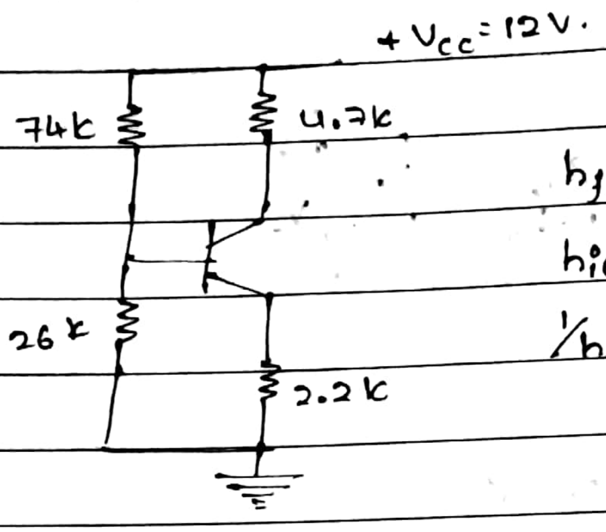
$= 5.98\ k\Omega$ //

(iii) $A_v = \dfrac{-h_{fe}}{h_{ie}} [R_c \parallel 1/h_{oe}] = -269.1$

iv) $A_I = \dfrac{h_{fe}(R_1 \parallel R_2)}{[h_{ie} + (R_1 \parallel R_2)]} =$

Date : / /
Page No.:

2).



$h_{fe} = 100$

$h_{ie} = 1.2k$

$1/h_{oe} = 50k.$

i) $Z_i = h_{ie} \parallel (R_1 \parallel R_2)$

$= (1.2\times10^3) \parallel \left(\frac{74\times26}{100}\right).$

$= (1.2) \parallel (19.24)$

$= \frac{(1.2)(19.24)}{(1.2+19.24)}$

$= 1.129\ k\Omega$ //

ii) $Z_o = R_C \parallel (1/h_{oe})$

$= 4.7 \parallel (50)$

$= \frac{(4.7)(50)}{54.7}$

$= 4.296 k\Omega$ //

Date : / /
Page No.:

iii) $A_v = \cancel{-h_{fe}}\ -h_f$

$$-\frac{h_{fe}}{h_{ie}}(R_c \parallel 1/h_{oe})$$

$$= -\frac{100}{1.2k}(4.296k)$$

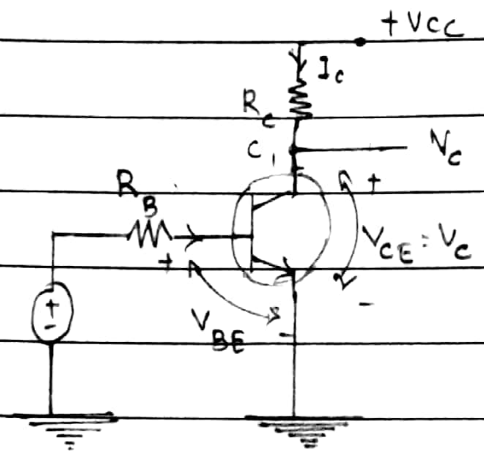
$$= -358$$

iv) $A_i =$

07/09/2017

Date : / /
Page No.:

BJT as a switch.



case 1: $V_i < 0.5V$, $\Rightarrow I_B = 0 \Rightarrow I_c = 0 \Rightarrow$ BJT is cutoff

$\therefore V_C = V_{CE}$

* Node C

case 2:

$V_i > 0.5V$.

now base current (I_B) starts flowing & hence collector current I_c also starts flowing now. BJT is working in active region.

apply KVL to i/p. ckt.

$V_i = I_B R_B + V_{BE}$

$$\boxed{I_B = \frac{V_i - V_{BE}}{R_B}} \quad \text{--- (1)}$$

$$\boxed{I_c = \beta I_B}$$

KVL to o/p loop.

$V_{cc} = I_c R_c + V_{CE}$ --- (2)

$$\therefore \boxed{V_{CE} = V_{cc} - I_c R_c} \quad \text{--- (3)}$$

Date : / /
Page No.:

case 3: when i/p volt. (V_i) is increased further so that BJT is just leaving the active region and entering into sat. region which we called as edge of saturation. (EOS)

Then. base current is denoted as I_{BEOS} collector current is denoted as I_{CEOS}.

KVL to o/p.

$$V_{IEOS} = I_{BEOS} R_B + V_{BE} \quad \text{——} ⓐ$$

then it's assume that when V_i is at EOS $V_{CEOS} = V_C$ is taken as 0.3V. so that I_{CEOS} can be obtained using,

$$I_{CEOS} = \frac{V_{CC} - V_{CEEOS}}{R_C} = \frac{V_{CC} - 0.3}{R_C} \quad \text{——} ⓑ$$

case 4:

when V_i is increased further BJT enters into sat. with the increased I_b and I_c values. It should be noted that under this condition $\boxed{V_{CEsat} = V_{C_{sat}} = 0.2V}$

then I_{csat} can be determined by: $I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C} \quad \text{——} ⓘ$

$$= \frac{V_{CC} - 0.2}{R_C} \quad \text{——} ⓘⓘ$$

I_B value is determined using eqn $\boxed{I_B = \frac{I_{csat}}{\beta}}$

Date : / /
Page No.:

when BJT is operated in sat. region the actual 'β' of which you can operate BJT can be ~~canged~~ changed to a lower value. So that we are forcing BJT to operate at lower 'β' value denoted β-force. & what amt it has to be decreased will be decided by overdrive factor denoted as 'ODF'. this value is decided by user and this is defined as ratio of actual 'β' to β-force

$$ODF = \frac{\beta}{\beta\ force}$$

also defined as ratio of I_b to I_{bEOS}

$$ODF = I_b / I_{bEOS}$$

when this ODF is given then after determining I_{csat} follo. procedure has to be followed.

v.imp

when ODF is given

$$I_{csat} = \frac{V_{cc} - 0.2}{R_c} \quad \text{— (a)}$$

$$I_{BEOS} = \frac{V_i - 0.3}{R_B} \quad \text{— (b)}$$

$$\beta_{forced} = \frac{\beta}{ODF} \quad \text{— (c)}$$

$$I_B = ODF \times I_{BEOS} \quad \text{— (d)}$$

Then $$R_B = \frac{V_I - V_{BE}}{I_B} \quad \text{— (e)}$$

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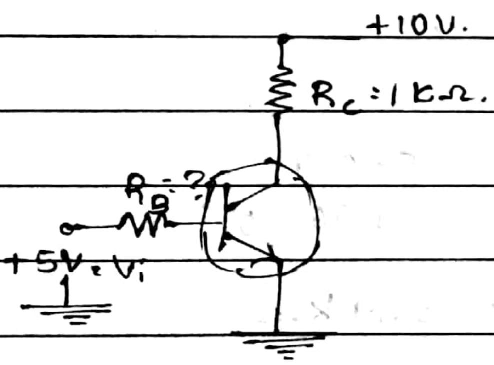
Date : / /
Page No.:

Hence, BJT is operated in deep sat region. Then we call this as BJT is ON and switch is closed but switch is closed by an offset volt of $V_{CEsat} = 0.2V$. i.e actually Node 'c' should be at 0V but in actual case $\boxed{V_{CE} = V_{CEsat} = 0.2V}$.

Problem:

1). The follo. transistor is specified to have β in the range of 50-150. design the value of R_B so that it operates BJT in sat. region with an ODF = 10.

Soln Given: β = 50 - 150, ODF = 10



Soln a) when i/p volt $V_i = 0V$ or say it's less than $V_i < 0.5V$. (silicon)

then $I_B = 0$, $I_C = 0$, BJT is off & switch is open.

b) ~~when~~ To operate BJT in sat. so that switch is closed we have to assume $V_{CEsat} = 0.2V$

Date:
Page No.:

$$I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C}$$

$$I_{Csat} = \frac{10 - 0.2}{1k} = 9.8mA$$

$$I_{BEOS} = \frac{I_{Csat}}{\beta}$$

(*) It is imp. to consider min. value of $\beta = 50$ to drive the transistor into saturation.

$$I_{BEOS} = \frac{9.8}{50} = 0.196\,mA$$

ODF is 10

$$\therefore \quad I_B = 10 \times 0.196\,mA$$
$$= 1.96\,mA$$

$$R_B = \frac{V_i - V_{BE}}{I_B} = \frac{5 - 0.7}{1.96 \times 10^{-3}}$$

$$= 2.19\,k\Omega$$

$$= 2.2\,k\Omega$$

$$\beta_{force} = \frac{50}{10} = \frac{\beta}{ODF}$$

$$\boxed{\beta_{force} = 5}$$

Date : / /
Page No.:

27. Consider, the ckt of BJT as a switch with $V_{cc} = +5V$, $V_i = +5V$, $R_B = R_C = 1k\Omega$ & $\beta = 100$ calculate the base current collector current and collector volt., if the trans. is saturated find $\beta_{forced} = ?$ what is the value of R_B to bring the trans to the edge of sat.

Sol^n: $V_{cc} = +5V$, $V_i = +5V$, $R_B = R_C = 1k\Omega$. $\beta = 100$.

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5-0.7}{1000} = 4.3mA$$

*) $$I_{Csat} = \frac{V_{cc} - V_{CEsat}}{R_C} = \frac{5-0.2}{1k} = 4.8mA$$

$$\beta_{force} = \frac{I_{Csat}}{I_B} = \frac{4.8mA}{4.3mA} = 1.12$$

*) $$ODF = \frac{\beta}{\beta_{force}} = \frac{100}{1.12} = 89.285$$

$\cancel{R_{BEOS} = I_{BEOS}}$ $$I_{CEOS} = \frac{V_{cc} - V_{CEOS}}{R_C} = \frac{5-0.3}{1000} = 4.7mA$$

$$I_{BEOS} = \frac{I_{CEOS}}{\beta} = \frac{4.7mA}{100} = 0.047mA.$$

$$R_{B_{EOS}} = \frac{V_i - V_{BE}}{I_{BEOS}} = \frac{5-0.7}{0.047 \times 10^{-3}} = 91.49 k\Omega = 91.5 k\Omega$$

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Date : / /
Page No :

14/09/17

~~Test 01~~

chap 03: MOSFET characteristics and it's

Types of MOSFET (Metal oxide Semiconductor field effect Transistor).

2 types

1) Depletion type

2) enhancement
   - N channel
   - P channel.

constr. diagram of

NMOSFET depletion type.

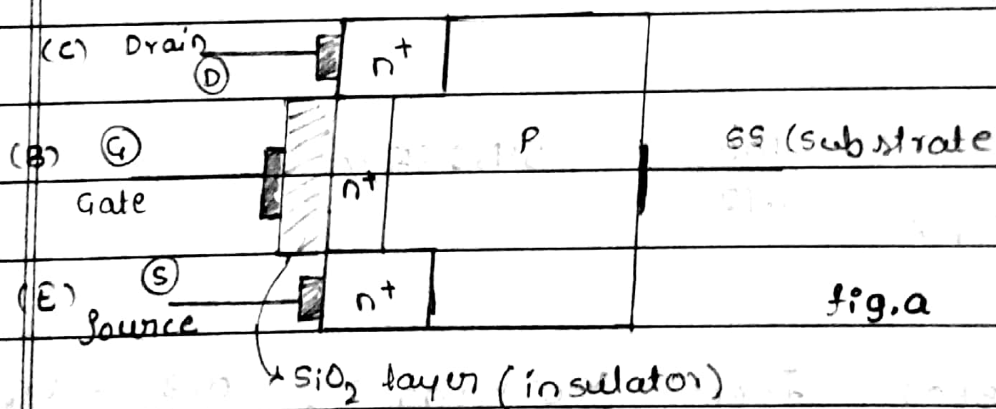


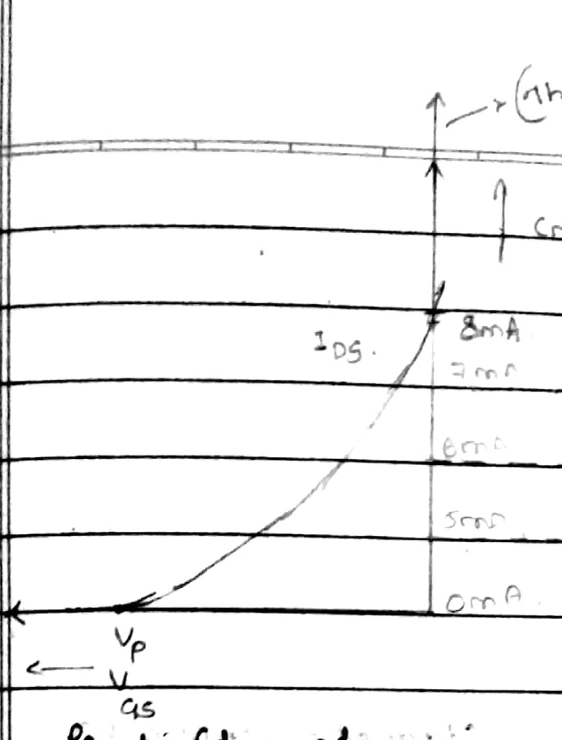
fig.a

1) when $V_G = 0V$
2) when $V_G = -ve$

} → depletion mode

3) when $V_G = +ve$.

Date : / /
Page No.:



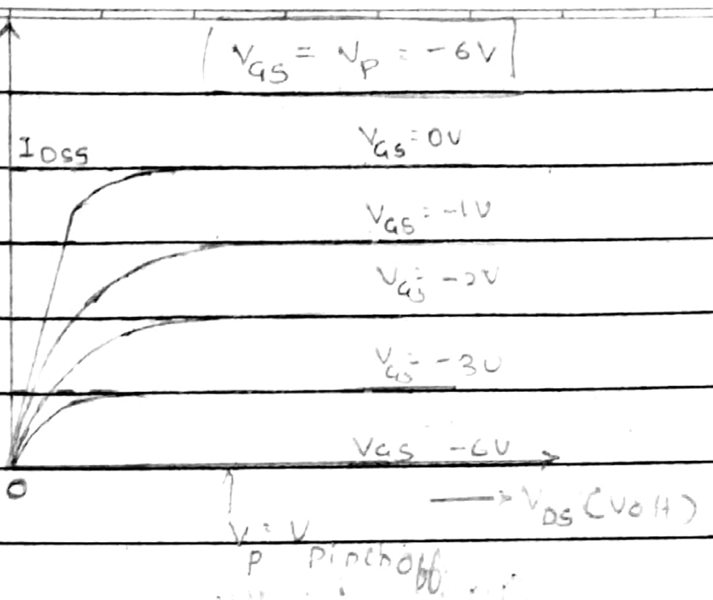
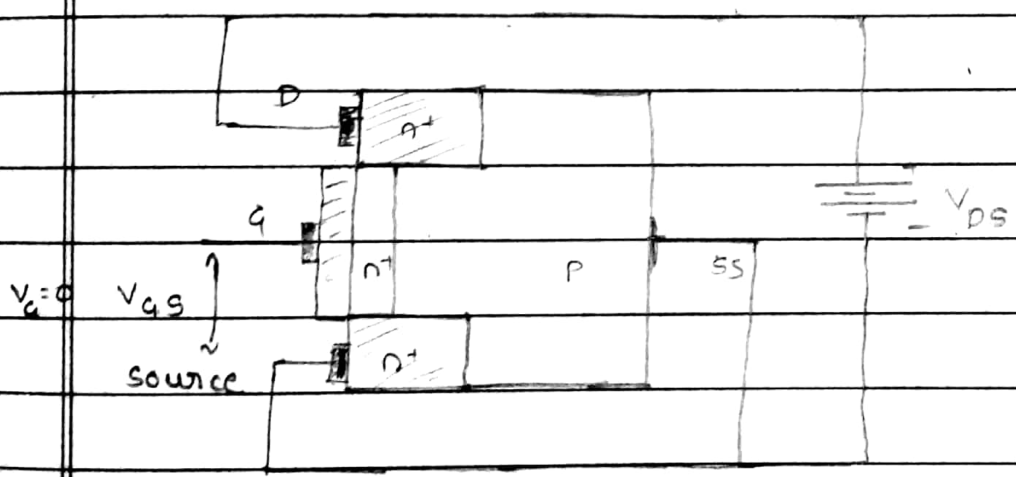


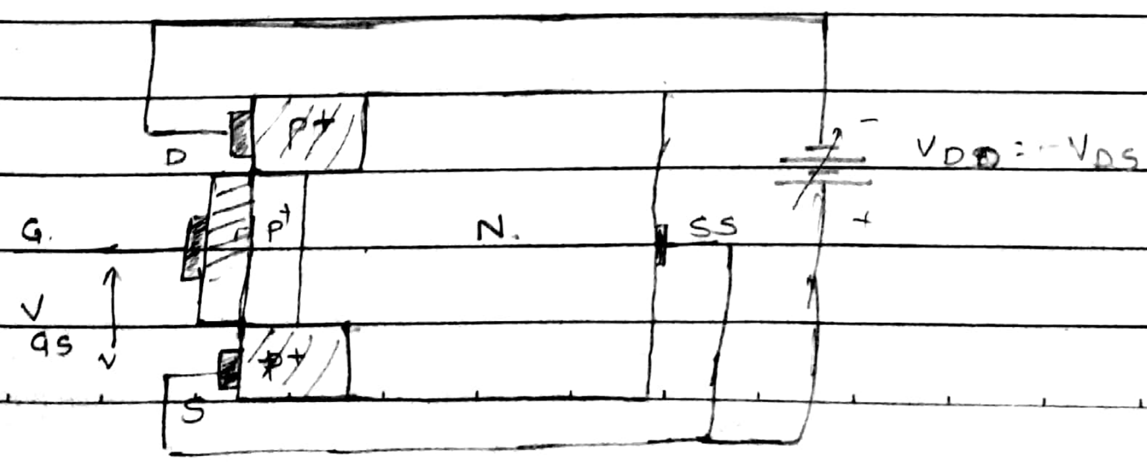
fig. b (transfer characteristics).

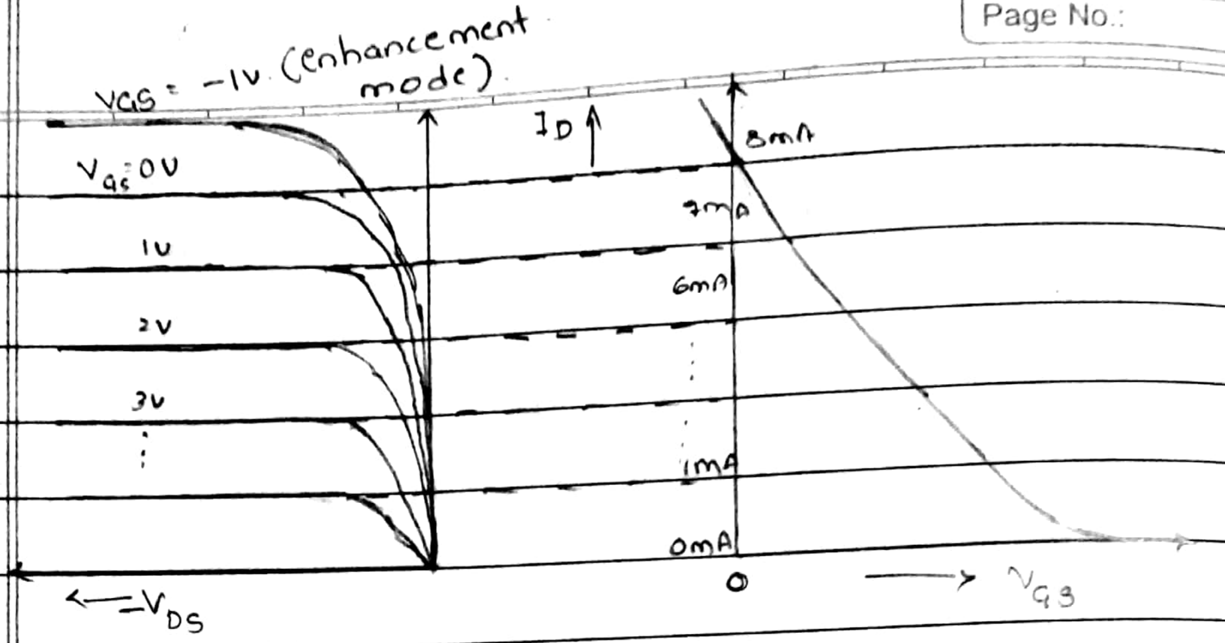
fig. c (Drain / o/p. char).

N-channel.



P-channel.





(Drain charact.)

(transfer charact.)